74HC138; 74HCT138

3-to-8 line decoder/de multiplexer; inverting

Rev. 4 — 27 June 2012 Product data sheet

1. General description

The 74HC138; 74HCT138 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC138; 74HCT138 decoder accepts three binary weighted address inputs (A0, A1 and A3) and when enabled, provides 8 mutually exclusive active LOW outputs ($\overline{Y0}$ to $\overline{Y7}$).

The 74HC138; 74HCT138 features three enable inputs: two active LOW ($\overline{E1}$ and $\overline{E2}$) and one active HIGH (E3). Every output is HIGH unless $\overline{E1}$ and $\overline{E2}$ are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the 74HC138; 74HCT138 to a 1-of-32 (5 lines to 32 lines) decoder with just four 74HC138; 74HCT138 ICs and one inverter.

The 74HC138; 74HCT138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Permanently tie unused enable inputs to their appropriate active HIGH- or LOW-state.

The 74HC138; 74HCT138 is identical to the 74HC238; 74HCT238 but has inverting outputs.

2. Features and benefits

- Demultiplexing capability
- Multiple input enable for easy expansion
- Complies with JEDEC standard no. 7A
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- ESD protection:
  - HBM EIA/JESD22-A114F exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from Š40 °C to +85 °C and from Š40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC138N	Š40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT138N				
74HC138D	Š40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74 HCT138D				
74HC138DB	Š40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT138DB				
74HC138PW	Š40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT138PW				
74HC138BQ	Š40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT138BQ				

4. Functional diagram

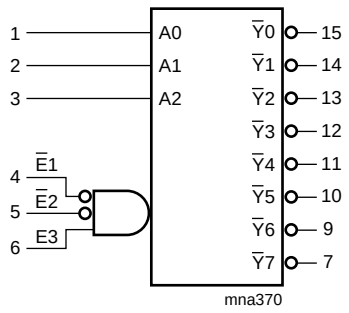

Fig 1. Logic symbol

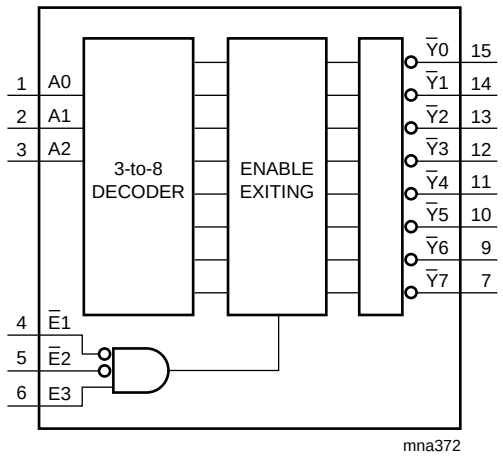

Fig 2. Functional diagram

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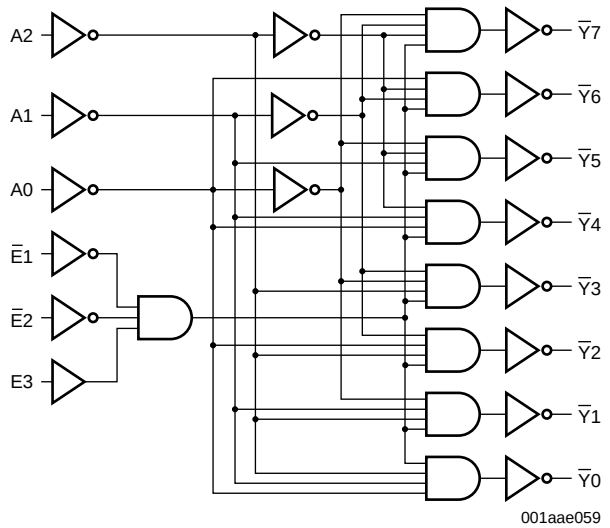


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

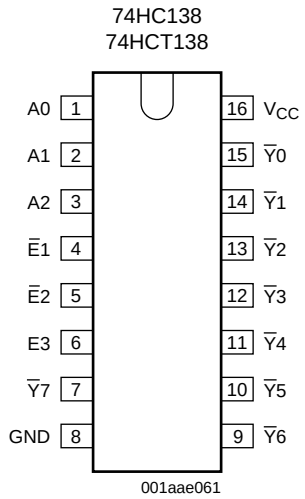
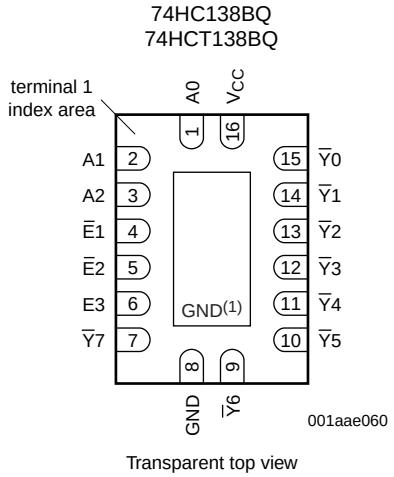


Fig 4. Pin configuration DIP16, SO16, SSOP16 and TSSOP16



(1) The die substrate is attached to this pad using conductive die attach material. It cannot be used as supply pin or input.

Fig 5. Pin configuration DHVQFN16

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5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0, A1, A2	1, 2, 3	address input A0, A1, A2
$\overline{E}1$, $\overline{E}2$	4, 5	enable input $\overline{E}1$, $\overline{E}2$ (active LOW)
E3	6	enable input E3 (active HIGH)
$\overline{Y}0$, $\overline{Y}1$, $\overline{Y}2$, $\overline{Y}3$, $\overline{Y}4$, $\overline{Y}5$, $\overline{Y}6$, $\overline{Y}7$	15, 14, 13, 12, 11, 10, 9, 7	output $\overline{Y}0$, $\overline{Y}1$, $\overline{Y}2$, $\overline{Y}3$, $\overline{Y}4$, $\overline{Y}5$, $\overline{Y}6$, $\overline{Y}7$ (active LOW)
GND	8	ground (0 V)
V_{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table [1]

Control			Input			Output							
$\overline{E}1$	$\overline{E}2$	E3	A2	A1	A0	$\overline{Y}7$	$\overline{Y}6$	$\overline{Y}5$	$\overline{Y}4$	$\overline{Y}3$	$\overline{Y}2$	$\overline{Y}1$	$\overline{Y}0$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X											
X	X	L											
L	L	H	L	L	L	H	H	H	H	H	H	H	L
			L	L	H	H	H	H	H	H	H	L	H
			L	H	L	H	H	H	H	H	L	H	H
			L	H	H	H	H	H	H	L	H	H	H
			H	L	L	H	H	H	L	H	H	H	H
			H	L	H	H	H	L	H	H	H	H	H
			H	H	L	H	L	H	H	H	H	H	H
			H	H	H	L	H	H	H	H	H	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		Š0.5	+7	V
I_{IK}	input clamping current	V_I < Š0.5 V or V_I > V_{CC} + 0.5 V	-	±20	mA
I_{OK}	output clamping current	V_O < Š0.5 V or V_O > V_{CC} + 0.5 V	-	±20	mA
I_O	output current	V_O = Š0.5 V to (V_{CC} + 0.5 V)	-	±25	mA
I_{CC}	quiescent supply current		-	50	mA
I_{GND}	ground current		-	Š50	mA
T_{stg}	storage temperature		Š65	+150	°C

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Table 4. Limiting values …continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation					
	DIP16 package		[1]	-	750	mW
	SO16 package		[2]	-	500	mW
	SSOP16 package		[3]	-	500	mW
	TSSOP16 package		[3]	-	500	mW
	DHVQFN16 package		[4]	-	500	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC138			74HCT138			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		Š40	+25	+125	Š40	+25	+125	°C
t/ V	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = Š40 °C to +85 °C		T_{amb} = Š40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC138										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V

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Table 6. Static characteristics …continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = Š40 °C to +85 °C		T_{amb} = Š40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = Š20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = Š20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = Š20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = Š4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = Š5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	per input pin; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; other inputs at V_{CC} or GND; V_{CC} = 6.0 V; I_O = 0 A		-	-	±0.5	-	±5.0	-	±10
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-					pF
74HCT138										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = Š20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = Š4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	per input pin; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; other inputs at V_{CC} or GND; V_{CC} = 5.5 V; I_O = 0 A		-	-	±0.5	-	±5.0	-	±10
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA

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Table 6. Static characteristics …continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		T_{amb} = −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	additional supply current	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		per input pin; An inputs	-	150	540	-	675	-	735	μA
		per input pin; $\overline{En}$ inputs	-	125	450	-	562.5	-	612.5	μA
		per input pin; E3 input	-	100	360	-	450	-	490	μA
C_I	input capacitance		-	3.5	-					pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		T_{amb} = −40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
For type 74HC138											
t_{pd}	propagation delay	An to $\overline{Yn}$; see Figure 6	[1]								
		V_{CC} = 2.0 V		-	41	150	-	190	-	225	ns
		V_{CC} = 4.5 V		-	15	30	-	38	-	45	ns
		V_{CC} = 5 V; C_L = 15 pF		-	12	-	-	-	-	-	ns
		V_{CC} = 6.0 V		-	12	26	-	33	-	38	ns
		E3 to $\overline{Yn}$; see Figure 6	[1]								
		V_{CC} = 2.0 V		-	47	150	-	190	-	225	ns
		V_{CC} = 4.5 V		-	17	20	-	38	-	45	ns
		V_{CC} = 5 V; C_L = 15 pF		-	14	-	-	-	-	-	ns
		V_{CC} = 6.0 V		-	14	26	-	33	-	38	ns
		$\overline{En}$ to $\overline{Yn}$; see Figure 7	[1]								
		V_{CC} = 2.0 V		-	47	150	-	190	-	225	ns
		V_{CC} = 4.5 V		-	17	20	-	38	-	45	ns
		V_{CC} = 5 V; C_L = 15 pF		-	14	-	-	-	-	-	ns
		V_{CC} = 6.0 V		-	14	26	-	33	-	38	ns
t_t	transition time	$\overline{Yn}$; see Figure 6 and Figure 7	[2]								
		V_{CC} = 2.0 V		-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V		-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V		-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC}	[3]	-	67	-	-	-	-	-	pF

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Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		T_{amb} = −40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
For type 74HCT138											
t_{pd}	propagation delay	An to $\overline{Y}$n; see Figure 6	[1]								
		V_{CC} = 4.5 V		-	20	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF		-	17	-	-	-	-	-	ns
		E3 to $\overline{Y}$n; see Figure 6	[1]								
		V_{CC} = 4.5 V		-	18	40	-	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF		-	19	-	-	-	-	-	ns
		$\overline{E}$n to $\overline{Y}$n; see Figure 7	[1]								
		V_{CC} = 4.5 V		-	19	40	-	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF		-	19	-	-	-	-	-	ns
t_t	transition time	$\overline{Y}$n; see Figure 6 and Figure 7	[2]								
		V_{CC} = 4.5 V		-	7	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC}	[3]	-	67	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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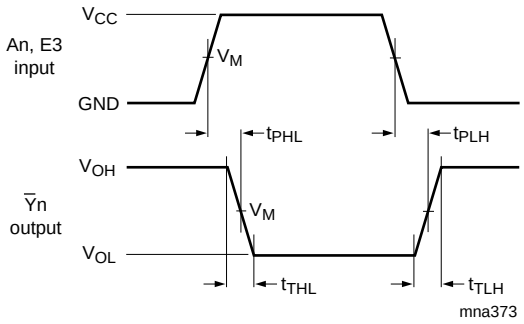
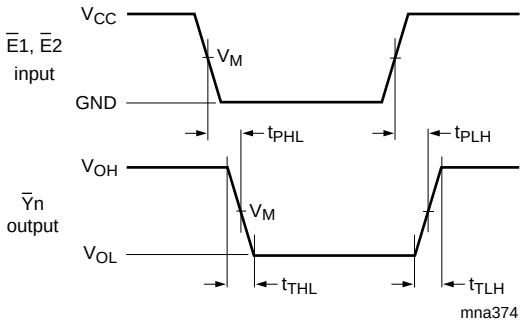
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay input (An) and enable input (E3) to output ($Y_{\overline{n}}$) and transition time output ($Y_{\overline{n}}$)



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Propagation delay enable input ($E_{\overline{n}}$) to output ($Y_{\overline{n}}$) and transition time output ($Y_{\overline{n}}$)

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC138	$0.5V_{CC}$	$0.5V_{CC}$
74HCT138	1.3 V	1.3 V

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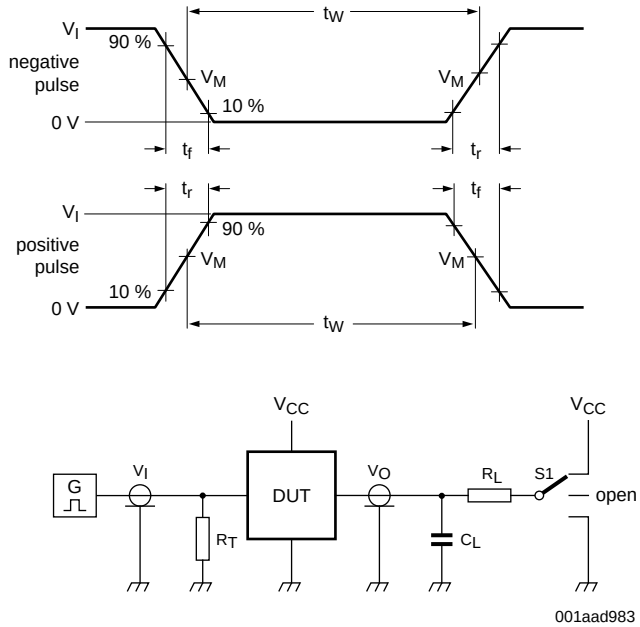

Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 8. Load circuitry for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC138	V_{CC}	6 ns	15 pF, 50 pF	1 k	open	GND	V_{CC}
74HCT138	3 V	6 ns	15 pF, 50 pF	1 k	open	GND	V_{CC}

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