LR1262 LoRaWAN Node Module DataSheet

V1.0

Table of Contents

1 Overview

1.1 Description

The LR1262 node module incorporates the SiP chip STM32WLE5CCU6, which is a SoC integrating the LoRa® RF and MCU chip combination. It embeds an ultra-low-power ARM Cortex-M4 MCU and the LoRa® SX126X. This module supports various communication modes, including (G)FSK modulation and LoRa® spread spectrum communication technology, thus meeting communication requirements in different scenarios.In LoRa communication mode, the module supports P2P communication and also has seamless connectivity with LoRaWAN networks. It can easily connect to mainstream LoRaWAN server platforms such as The Things Network (TTN) to achieve efficient data transmission between devices and the cloud.

The module provides users with a rich set of peripheral interfaces, including UART, I2C, SPI, ADC, and GPIO, which can meet a variety of hardware extension requirements. Through the UART interface, users can flexibly configure the communication mode and operational parameters of the module using AT commands. In addition, based on the STM32WLE5CCU6 microcontroller within the module, users can conduct software development and perform program erasure and programming via the SWD interface, thereby further enhancing the customizability and

application flexibility of the module.

1.2 Features

- Based on STM32WLE5CCU6
- Compliant with LoRaWAN 1.0.3 Specification
- Supports EU868 and US915 Frequency Bands
- LoRaWAN Activation via OTAA/ABP
- LoRa Point-to-Point (P2P) Communication
- Developed for Keil
- User-friendly AT Command Set via UART Interface
- Ultra-low Power Consumption of 1.69μA in Sleep Mode
- Operating Voltage: 2.0 V to 3.6 V
- Temperature Range: -40°C to 85°C

1.3 Applications

- Development of LPWAN Gateway Devices
- Development of Any Remote Wireless Communication Applications
- Learning and Research of LoRa® and LoRaWAN® Applications

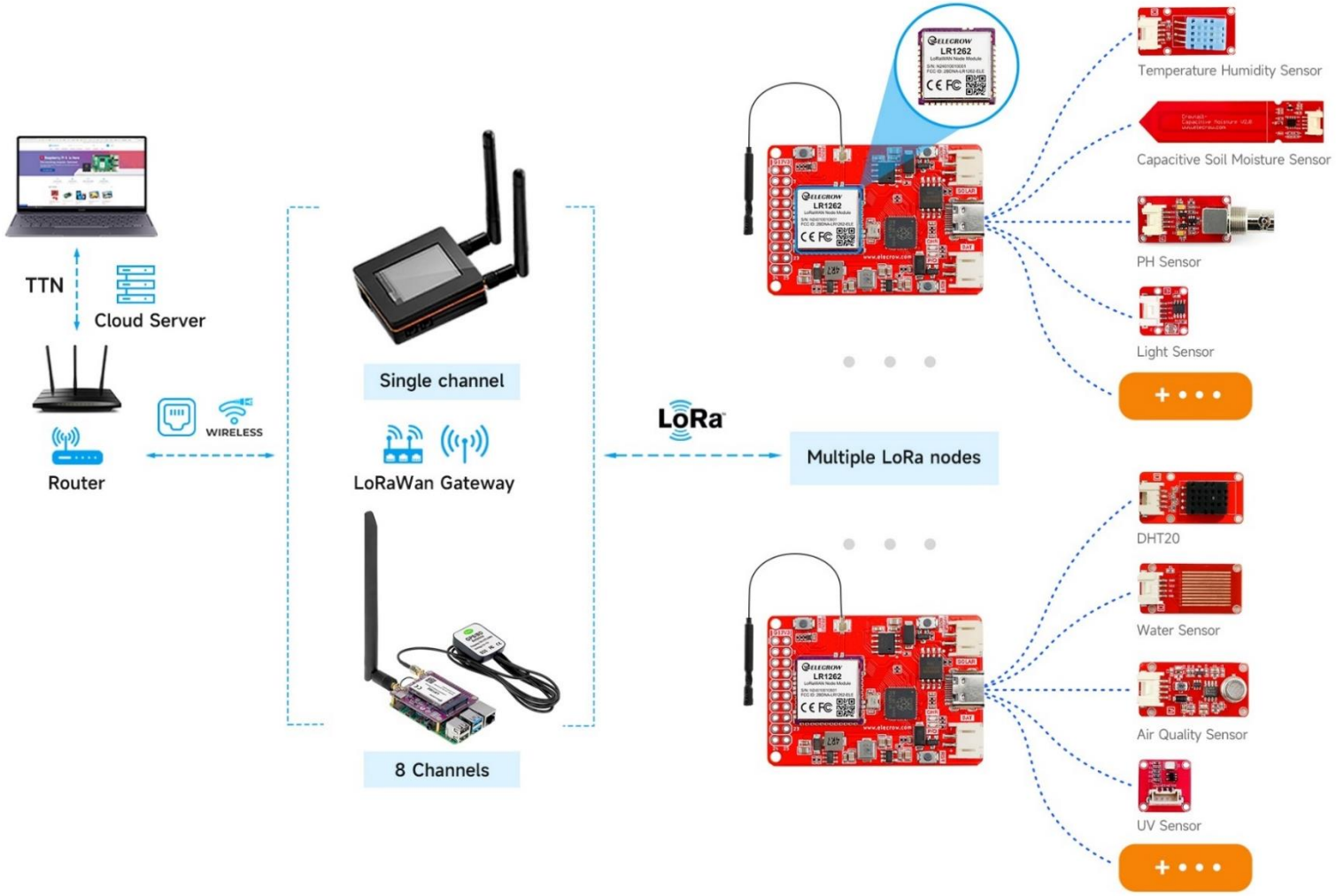

Figure 1 Network Topology Diagram

2 Product Appearance Diagram

Figure 2 Front View

Figure 3 Right View

Figure 4 Rear View

3 Dimension Drawing

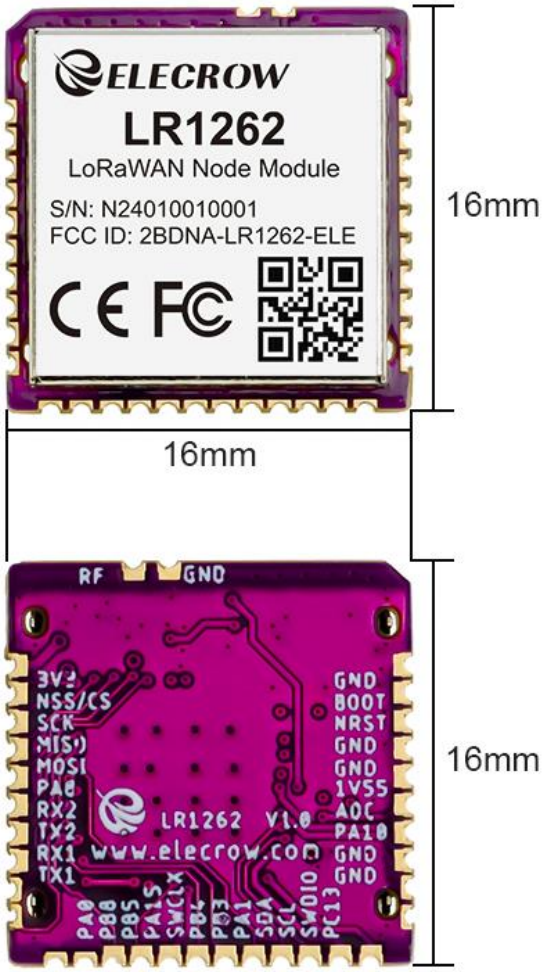

Figure 5 Dimension Drawing

4 System Block Diagram

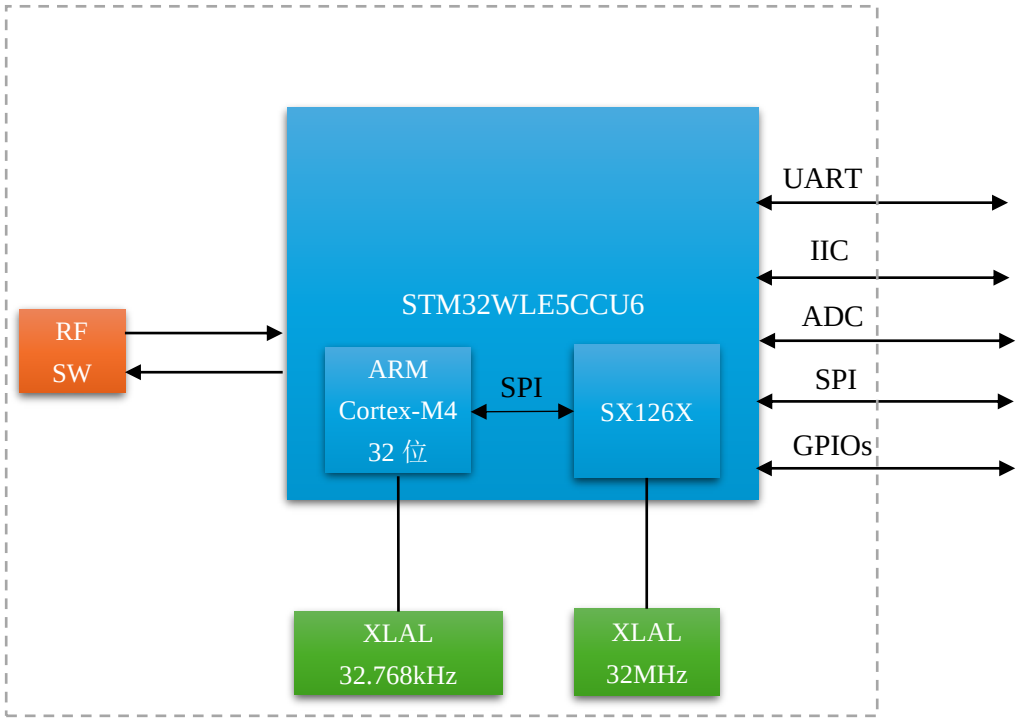

Figure 6 System Block Diagram

5 Technical Specifications

No.	Category	Item	Parameter
1	MCU	Processor	STM32WLE5CCU6（ARM Cortex-M4 32-bit）
2		RAM	64KB
3		Flash	256KB(with ECC)
4	RF Characteristics	RF Chip	SX1262
5		TX Transmission Power	20dBm@Max（868/915MHz）
6		RX Sensitivity	-123 dBm for 2-FSK(at 1.2 Kbit/s) -148 dBm for LoRa®(at 10.4 kHz, spreading factor 12)
7		LoRaWAN® Protocol	Class A/B/C (compliant with LoRaWAN 1.0.3 specification)
8		Supported Bands	EU8685、US915
9		Frequency Range	150 MHz to 960 MHz
10		Airspeed	0.018~62.5 Kbit/s
11		signal modulation	LoRa®、（G）FSK、（G）MSK 、BPSK
12		Communication Distance	5~7 KM
13		Operating Voltage	3.3V
14	Mechanical Characteristics	Antenna Type	Supports stamp holes or IPEX antenna mounts
15		Packaging Type	32pin SMT, stamp hole, 32-pin, tight I/O port, for PCB SMT installation
16		Dimensions	15 * 15 * 2.5mm
17		Weight	3g
18	Interface	Communication Interface	UART/SPI
19		Peripheral interface	UART, I2C, SPI, ADC, GPIO

6 Hardware Overview

Hardware Overview discusses the pin layout of the LR1262 node module and its corresponding functions.

6.1 LR1262 Node Module Pin Definition

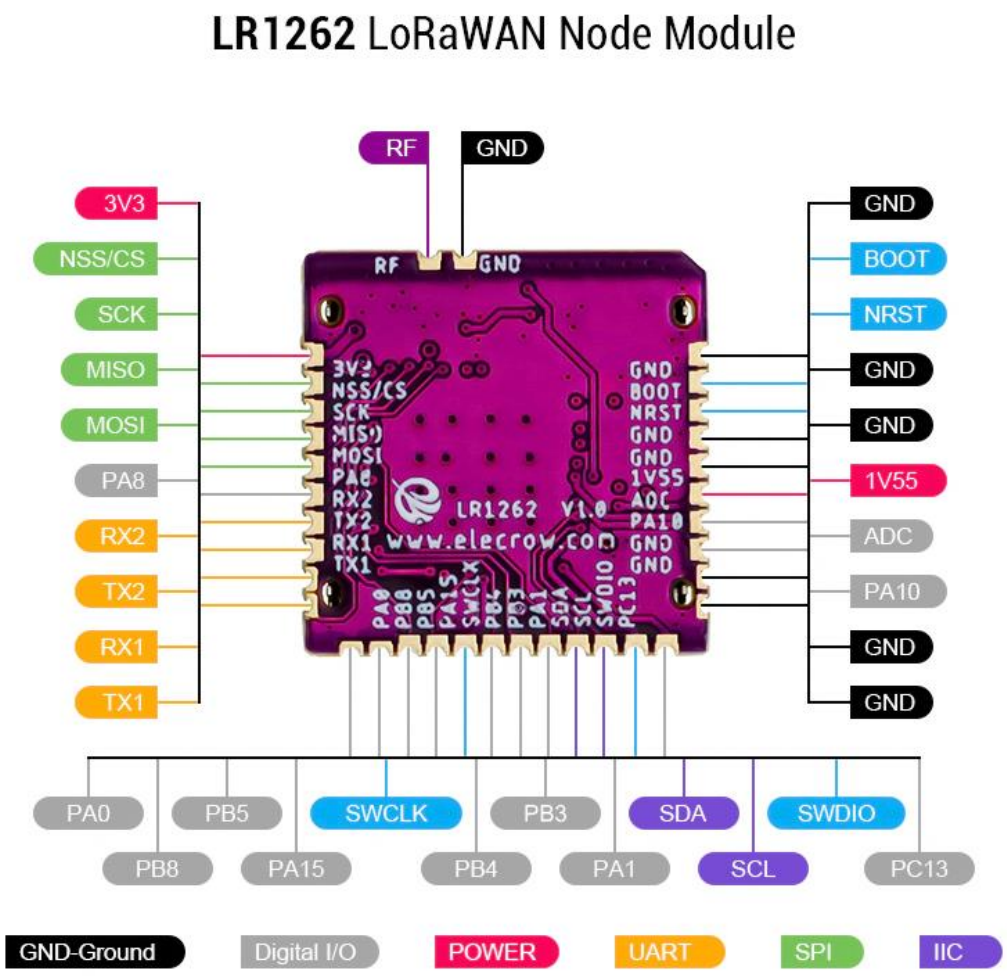

Figure 7 LR1262 Pin Definition Diagram

The following table provides the functional definitions and descriptions of the 32-pin gold-finger pins corresponding to the LR1262 node module.

Type	Description
IO	Bidirectional Input/Output
DI	Digital Input
DO	Digital Output
PI	Power Input

No.	Name	Type	Description
1	GND	GND	Ground
2	BOOT	I/O	Power On
3	NRST	I/O	Reset
4	GND	GND	Ground
5	GND	GND	Ground
6	1V55		Power Input 1.55V
7	ADC (PB2)	I/O	ADC
8	PA10	I/O	GPIO
9	GND		Ground
10	GND		Ground
11	PC13	I/O	
12	SWDIO(PA13)	I/O	SWD Debug Pin
13	SCL(PA12)	I/O	I2C（SCL）
14	SDA(PA11)	I/O	I2C（SDA）
15	PA1	I/O	GPIO
16	PB3	I/O	GPIO
17	PB4	I/O	GPIO
18	SWCLK(PA14)	I/O	SWD Debug Pin
19	PA15	I/O	GPIO
20	PB5	I/O	GPIO

21	PB8	I/O	GPIO
22	PA0	I/O	GPIO
23	TX1(PA2)	I/O	UART1 Interface
24	RX1(PA3)	I/O	UART1 Interface
25	TX2(PB6)	I/O	UART2 Interface
26	RX2(PB7)	I/O	UART2 Interface
27	PA8	I/O	GPIO
28	MOSI(PA7)	I/O	SPI（MOSI）
29	MISO(PA6)	I/O	SPI（MISO）
30	SCK(PA5)	I/O	SPI（SCK）
31	NSS/CS(PA4)	I/O	SPI（CS）
32	3V3(VDD)	Supply pin	Power Input 3.3V

6.2 STM32WLE5CCU6 Chip Pin Functions

No.	Pin	Type	Alternate Function	Additional Function
1	GND	GND		
2	BOOT	I/O	CM4_EVENTOUT	
3	NRST	I/O		
4	GND	GND		
5	GND	GND		
6	1V55			
7	ADC (PB2)	I/O	LPTIM1_OUT,I2C3_SMBA,SPI1_NSS,DEBUG_RF_SMPSRDY	COMP1_INP,COMP2_INM,ADC_IN4
8	PA10	I/O	RTC_REFIN,TIM1_CH3,I2C1_SDA,SPI2_MOSI/I2S2_SD,USART1_RX,DEBUG_RF_HSE32RDY,TIM17_BKIN,SM4_EVENTOUT	COMP1_INM,COMP2_INM,DAC_OUT1,ADC_IN6
9	GND			
10	GND			
11	PC13	I/O	CM4_EVENTOUT	TAMP_IN1/RTC_OUT1/RTC_TS/WKUP2
12	SWDIO (PA13)	I/O	JTMS-SWDIO,I2C2_SMBA	ADC_IN9
13	SCL	I/O	TIM1_ETR,LPTIM3_IN1,I2C2_SCL,SPI1_MOS	ADC_IN8

	(PA12)		I,RF_BUSY,USART1_RTS,CM4_EVENTOUT	
14	SDA (PA11)	I/O	TIM1_CH4,TIM1_BKIN2,LPTIM3_ETR,I2C2_SDA,SPI1_MISO,USART1_CTS,DEBUG_RF_NRESET	COMP1_INM,COMP2_INM,ADC_IN7
15	PA1	I/O	TIM2_CH2,LPTI3_OUT,I2C1_SMBA,SPI1_SCK,USART2_RTS,LPUART1_RTS,DEBUG_PWR_REGLP2S,CM4_EVENTOUT	
16	PB3	I/O	JTD0/TRACESWO,TIM2_CH2,SPI1_SCK,RF_IRQO,USART1_RTS,DEBUG_RF_DTB1,CM4_EVENTOUT	COMP1_INM,COMP2_INM,ADC_IN2,TAMP_IN3/WKUP3
17	PB4	I/O	NJTRST,I2C3_SDA,SPI1_MISO,USART1_CTS,DEBUG_RF_LDORDY,TIM17_BKIN	COMP1_INP,COMP2_INP,ADC_IN3
18	SWCLK (PA14)	I/O	JTCK-SWCLK,LPTIM1_OUT,I2C1_SMBA,CM4_EVENTOUT	ADC_IN10
19	PA15	I/O		
20	PB5	I/O	LPTIM1_IN1,I2C1_SMBA,SPI1_MOSI,RF_IRQ1,USART1_CK,COMP2_OUT,TIM16_BKIN	
21	PB8	I/O	TIM1_CH2N,I2C1_SCL,RF_IRQ2,TIM16_CH1,CM4_EVENTOUT	
22	PA0	I/O	TIM2_CH1,I2C3_SMBA,I2S_CKIN,USART2_CTS,COMP1_OUT,DEBUG_PWR_REGLP1S,TIM2_ETR	TAMP_IN2/WKUP1
23	TX1 (PA2)	I/O	LSCO,TIM2_CH3,USART2_TX,LPUART1_TX,COMP2_OUT,DEBUG_PWR_LDORDY	LSCO
24	RX1 (PA3)	I/O	TIM2_CH4,I2S2_MCK,USART_RX,LPUART1_RX,CM4_EVENTOUT	
25	TX2 (PB6)	I/O	LPTIM1_ETR,I2C1_SCL,USART1_TX,TIM16_CH1N	
26	RX2 (PB7)	I/O	LPTIM1_IN2,TIM1_BKIN,I2C1_SDA,USART1_RX,TIM17_CH1N	
27	PA8	I/O	MCO,TIM1_CH1,SPI2_SCK/I2S2_CK,USART1_CK,LPTIM2_OUT	
28	MOSI (PA7)	I/O	TIM1_CH1N,I2C3_SCL,SPI1_MOSI,COMP2_OUT,DEBUG_SUBGHZSPI_MOSIOUT,TIM17_CH1,CM4_EVENTOUT	
29	MISO (PA6)	I/O	TIM1_BKIN.I2C2_SMBA,SPI1_MISO,LPUART1_CTS,DEBUG_SUBGHZSPI_MISOOUT,TIM16_CH1,CM4_EVENTOUT	
30	SCK (PA5)	I/O	TIM2_CH1,TIM2_ETR,SPI2_MISO,SPI1_SCK,DEBUG_SUBGHZSPI_SCKOUT,LPTIM2_ETR,CM4_EVENTOUT	

31	NSS/CS (PA4)	I/O	RTC_OUT2,LPTIM1_OUT,SPI1_NSS,USART2_CK,DEBUG_SUBGHZSPI_NSSOUT,LPTIM2_OUT,CM4_EVENTOUT	
32	3V3 (VDD)	Supply pin		
33	RF	ANT		
34	GND	GND		

7 Interfaces

7.1 Power Interface

No.	Power Supply Pin	Pin Number	Pin Type	Function Description
1	3V3-VDDRF	P$26	PI	3.3V RF power supply input
2	VDDRF1V55	P$1	PI	1.55V RF power supply input
3	GND	P$4,P$27,P$28, P$29,P$33,P$34	PI	Ground

7.2 UART Interface

No.	UART Interface Signal	Pin Number	Pin Type	Function Description	Voltage Domain
1	UART1-TX	P$17	I/O	General-purpose asynchronous transmit pin for UART1 transmission	3.3V
2	UART1-RX	P$18	I/O	General-purpose asynchronous receive pin for UART1 reception	3.3V
3	LPUART1-TX	P$19	I/O	Low-power general-purpose asynchronous transmit pin for LPUART1 transmission	3.3V
4	LPUART1-RX	P$20	I/O	Low-power general-purpose asynchronous receive pin for LPUART1 reception	3.3V

7.3 SPI Interface

No.	SPI Interface Signal	Pin Number	Pin Type	Function Description	Voltage Domain
1	SPI_NSS/CS	P$25	I/O	Chip select signal input, used to select SPI device	3.3V
2	SPI_SCK	P$24	I/O	SPI clock signal input	3.3V
3	SPI_MISO	P$23	I/O	SPI data output	3.3V
4	SPI_MOSI	P$22	I/O	SPI data input	3.3V

7.4 I2C Interface

No.	I2C Interface Signal	Pin Number	Pin Type	Function Description	Voltage Domain
1	I2C_SCL	P$7	I/O	I2C clock line, used for I2C communication clock signal	3.3V
2	I2C_SDA	P$8	I/O	I2C data line, used for I2C communication data transfer	3.3V

7.5 ADC Interface

No.	ADC Interface Signal	Pin Number	Pin Type	Function Description	Voltage Domain
1	ADC	P$2	I/O	Analog-to-digital converter pin, used for digitizing analog signals	3.3V

7.6 SWD Debug Interface

No.	Debug Interface Signal	Pin Number	Pin Type	Function Description	Voltage Domain
1	SWDIO	P$6	I/O	Debug and programming interface pin, used for data transmission	3.3V
2	SWCLK	P$12	I/O	Debug and programming interface pin, used for transmitting clock signals (synchronizing data)	3.3V

7.7 GPIOs Interface

No.	IO Interface Signal	Pin Number	Pin Type	Function Description	Voltage Domain
1	PA0	P$25	I/O	Data input and output	3.3V
2	PA1	P$24	I/O		3.3V
3	PA10	P$3	I/O		3.3V
4	PA15	P$23	I/O		3.3V
5	PB3	P$22	I/O		3.3V
6	PB4	P$11	I/O		3.3V
7	PB5	P$14	I/O		3.3V
8	PB8	P$15	I/O		3.3V
9	PB15	P$13	I/O		3.3V
10	PC13	P$5	I/O		3.3V

8 Electrical Characteristics

8.1 Power Consumption

NO.	Mode	Minimum	Typical	Maximum
1	TX Current	/	87 mA@20dBm 868Mhz	/
2	RX Current	/	5.2 mA	/
3	Minimum Sleep Current	1.69μA	/	2.0μA

9 Environmental Characteristics

9.1 Extreme Operating Conditions

NO.	Item	Description	Minimum	Maximum	Unit
1	VCCmr	Supply Voltage	1.71	3.6	V
2	Tmr	Ambient Temperature	-40	+85	℃

9.2 Normal Operating Conditions

NO.	Item	Description	Minimum	Maximum	Unit
1	VCCop	Supply Voltage	1.8	3.0	V
2	Top	Ambient Temperature	-30	+85	℃

10 Application Information

10.1 Package Information

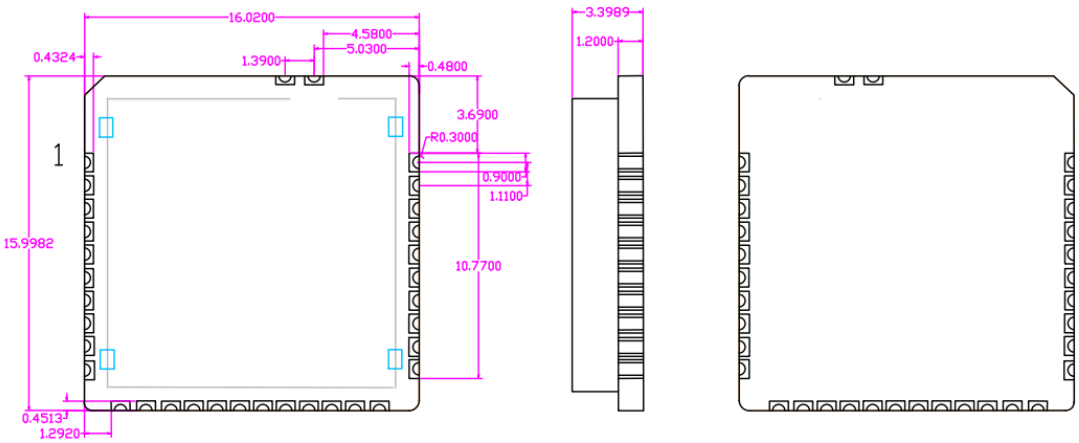

Figure 8 Package Outline Drawing (Unit:mm)

10.2 Land Pattern

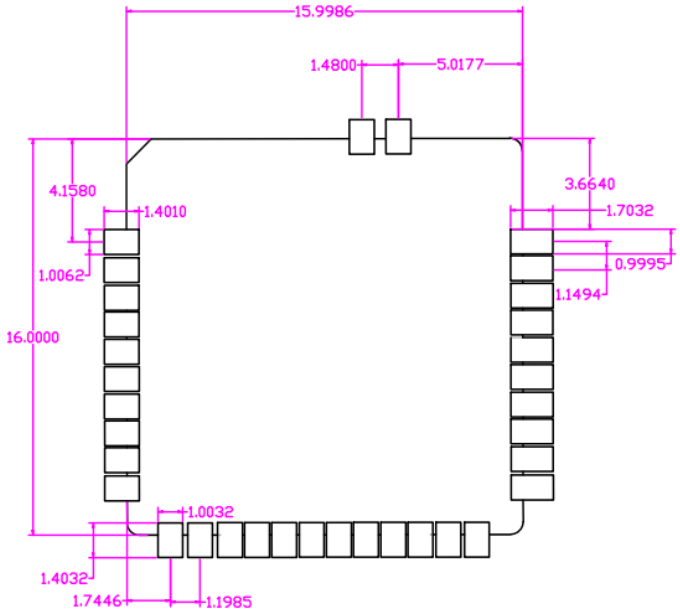

Figure 9 PCB Layout (Unit:mm)

10.3 Package Marking

Figure 10 Package Marking Diagram

11 Certifications

12 Related Documents and Ordering Information

12.1 Related Documents

- **LR1262 LoRaWAN Node Module Product Link**
- **LR1262 LoRaWAN Node Module WIKI**
- **LR1262 LoRaWAN AT Command Description**
- **SX1261/2 Datasheet**

12.2 Ordering Information

Sku	Product Name	Product Image
CRT01268N	LR1262 LoRaWAN Node Module	
CRT01269N	LR1262 Node Board	
CRT01267D	LoRaWAN LR1262 Development Board	
CRT01158H	Crowtail- LoRaWAN Lora RA-08H/LR1262 Module	

13 Revision History

Date	Version	Release Notes
2025/4/18	V1.0	Initial Release