

- Tentative Specification
- Preliminary Specification
- Specification Approval

Specification For SID 4.20” BW EPD

Model Name: SE0420NQN42-MNG-A0

Version:V0.1

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	Notes:	

Notes :

- 1、 Please contact SID before assigning your product based on this module specification.
- 2、 To improve the quality of product, and this product specification is subject to change without any notice.

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1 General Description

SE0420NQN42-MNG-A0 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The 4.2" active area contains 400x300 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2 Features

- ◆ 400×300pixels display
- ◆ White reflectance above 30%
- ◆ Contrast ratio above 8:1
- ◆ Ultra wide viewing angle
- ◆ Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Landscape, portrait modes
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform stored in On-chip OTP
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I2C signal master interface to read external temperature sensor

3 Application

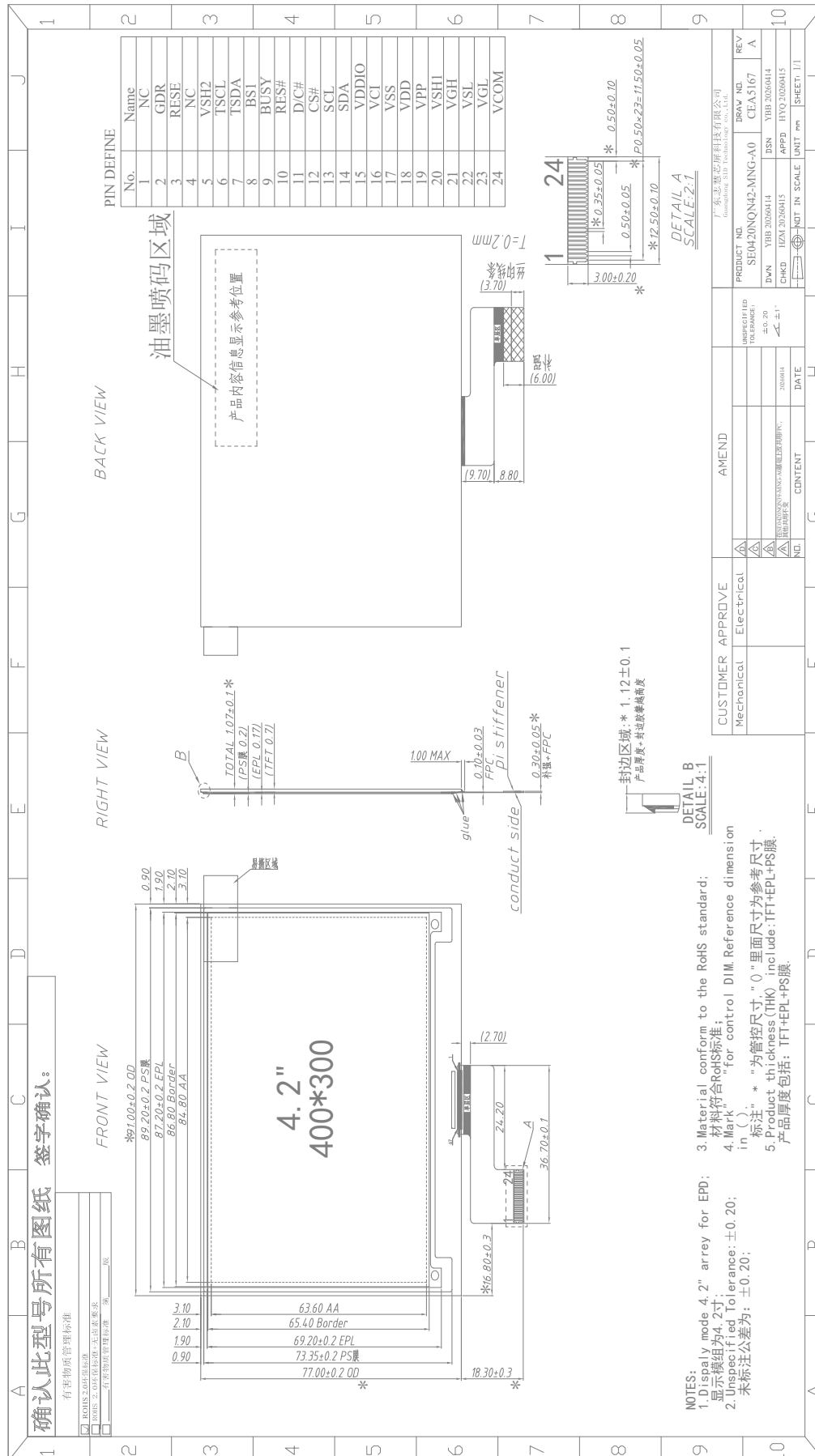
Electronic Shelf Label System or others

4 Mechanical Specification

4.1 Dimension

Parameter	Specifications	Unit
Screen Size	4.2	Inch
Display Resolution	400(H)×300(V)	Pixel
Active Area	84.80×63.60	mm
Pixel Pitch	0.212×0.212	mm
Pixel Configuration	Square	
Outline Dimension	91.00(H)×77.00(V) ×1.07(D)	mm

4.2 Mechanical Drawing of EPD Module



5 Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	
5	VDHR	C	Positive Source driving voltage 1	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS	I	Bus Interface selection pin	Note 5-4
9	BUSYN	O	Busy state output pin	Note 5-3
10	RSTN	I	Reset signal input. Active Low.	
11	D/C	I	Data /Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDD/VDDIO	P	Power Supply for interface logic pins	
16	VDD/VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDDD	C	Core logic power pin VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances	
19	VPP	P	Power Supply for OTP Programming	
20	VSH	C	Positive Source driving voltage	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent. For example. The chip would put Busy pin Low when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin

BS State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	Vdd	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to Vdd +0.5	V
Logic Output voltage	VOUT	-0.5 to Vdd +0.5	V

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VDD=3.0V, TOPR =25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Logic supply voltage	Vdd	-	VDD	2.3	3.0	3.6	V
High level input voltage	VIH	-	0.7VDDIO	-	VDDIO	-	V
Low level input voltage	VIL	-	0	-	-	0.3 Vdd	V
High level output voltage	VOH	IOH = 400uA	VDDIO-0.4	-	-	-	V
Low level output voltage	VOL	IOL = -400uA	0	-	-	0.4	V
Typical power panel	PTYP	-	-	-	4.5	-	mW
Deep sleep mode	PSTPY	-	-	-	3	-	uW
Typical operating current	Iopr_VDD	Vdd =3.0V-	-	-	3	-	mA

Sleep mode current	Islp_VDD	VDD=3.0V DC/DC OFF No clock No output load Ram data retain	VDD	-	27	--	uA
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Deep sleep mode current	IdslpVDD	VDD=3.0V DC/DC OFF No clock No output load Ram data not retain	VDD	-	1	--	uA
Operation temperature	TOPR	-	-	0	-	50	°C
Operation relative humidity	RHop	-	-	-	-	70	%RH
Operation illuminance intensity	E	indoor only	-	-	-	2000	lux

Notes: 1. The typical power is measured with following transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 10-2)

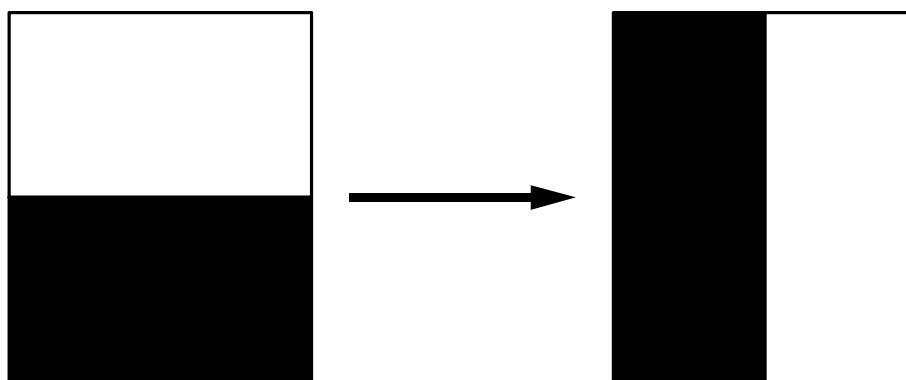


Figure 10-2 The typical power consumption measure pattern

- 2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
- 3..The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by SID.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VDD =3.0V, TOPR =25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM		-1.5		V

6.4 Panel AC Characteristics

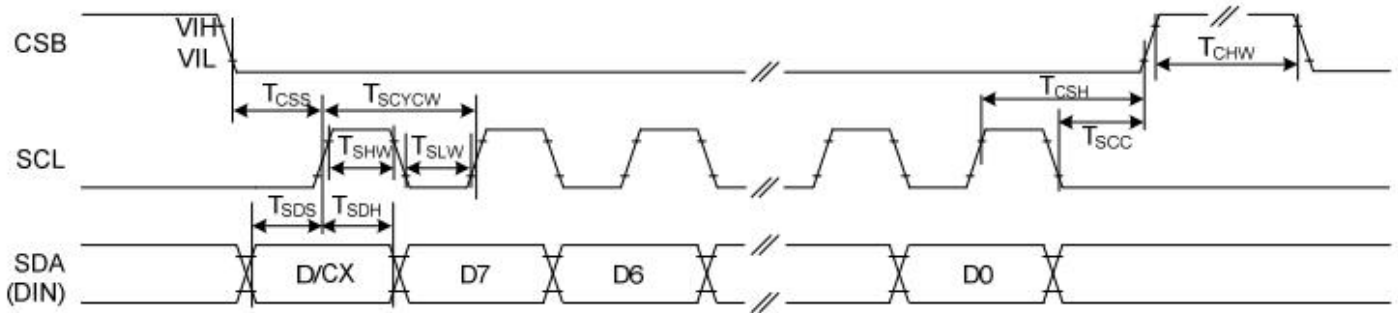


Figure: 3-wire Serial Interface Characteristics (Write mode)

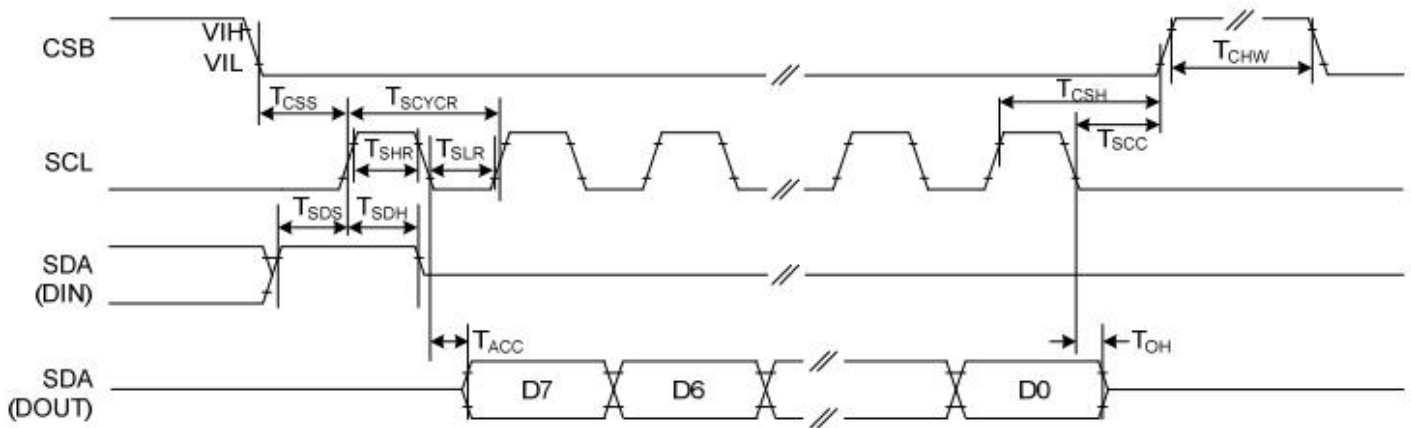
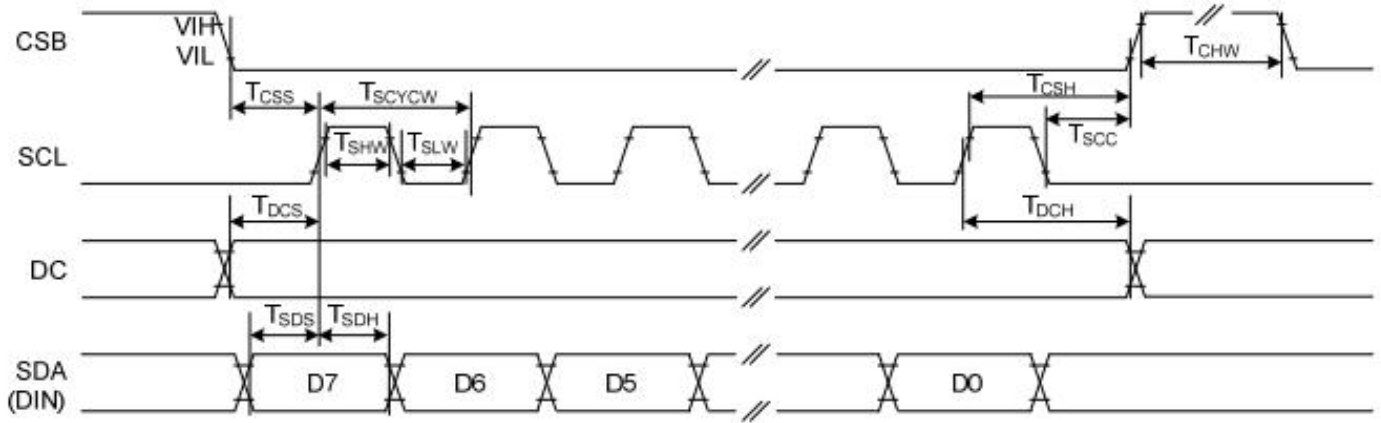
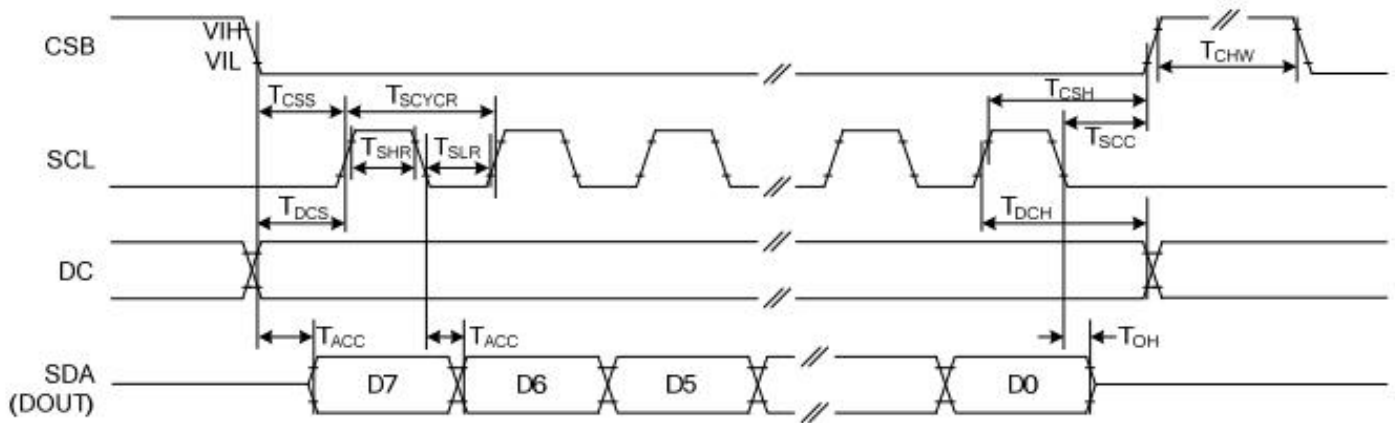


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL "H" pulse width (Write)	35			ns
T_{SLW}		SCL "L" pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL "H" pulse width (Read)	175			ns
T_{SLR}	SCL "L" pulse width (Read)	175			ns	
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA	Access time			250	ns
T_{OH}	SDA (DOUT)	Output disable time	15			ns


Figure: 4-wire Serial Interface Characteristics (Write mode)

Figure: 4-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL "H" pulse width (Write)	35			ns
T_{SLW}		SCL "L" pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}	SCL	SCL "H" pulse width (Read)	175			ns
T_{SLR}		SCL "L" pulse width (Read)	175			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA	Access time			250	ns
T_{OH}	SDA (DOUT)	Output disable time	15			ns

7 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

Symbol	Parameter	Conditions	Values			Units	Notes
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	11-1
CR	Contrast Ratio		6:1	8:1	-	-	11-2
White Δ L 24h	Reduce		-	≤ 4	-	-	-
Tupdate	Image update time	at25 °C (LUT_GC)	-	1000	-	ms	-
		at25 °C (LUT_DU)	-	500	-	ms	-

Notes: 11-1. Luminance meter: Eye-One Pro Spectrophotometer.

11-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

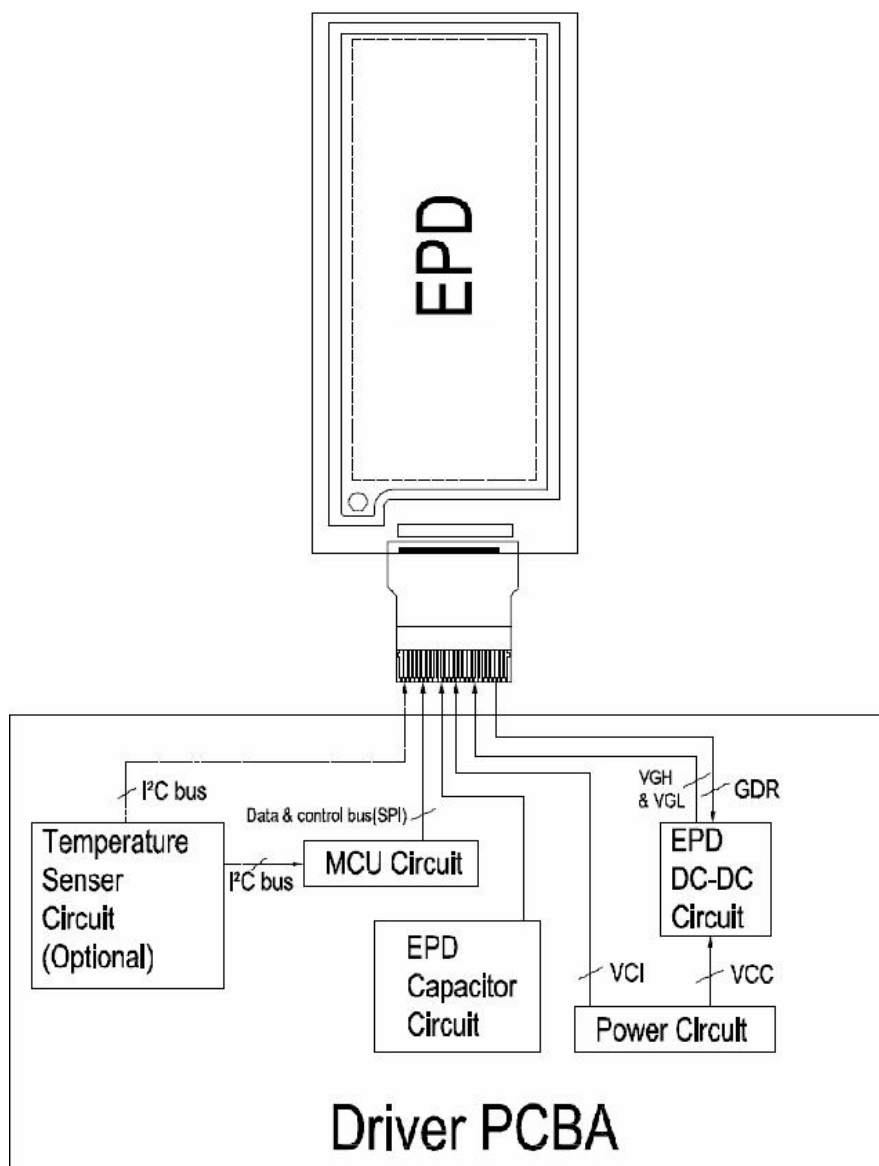
8 Handling, Safety, and Environment Requirements

1. The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel
2. The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
3. Do not apply pressure to the EPD panel in order to prevent damaging it
4. Do not connect or disconnect the interface connector while the EPD panel is in operation
5. Do not stack the EPD panels / Modules.
6. Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.
7. Do not disassemble or reassemble the EPD panel
8. Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet
9. Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation
10. It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.
11. High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package. Without sunlight, without condensation a temperature range of 15°C to 35°C, and humidity from 30%RH to 60%RH.

9 Reliability Test

No.	Test	Condition	Method	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
4	Low-Temperature Storage	T = -25°C for 240 hrs	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
6	High Temperature, High-Humidity Storage	T = +60°C, RH=80% for 240hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
7	Thermal Shock	1 cycle:[-25°C 30min]→[+70°C 30 min] : 100 cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.

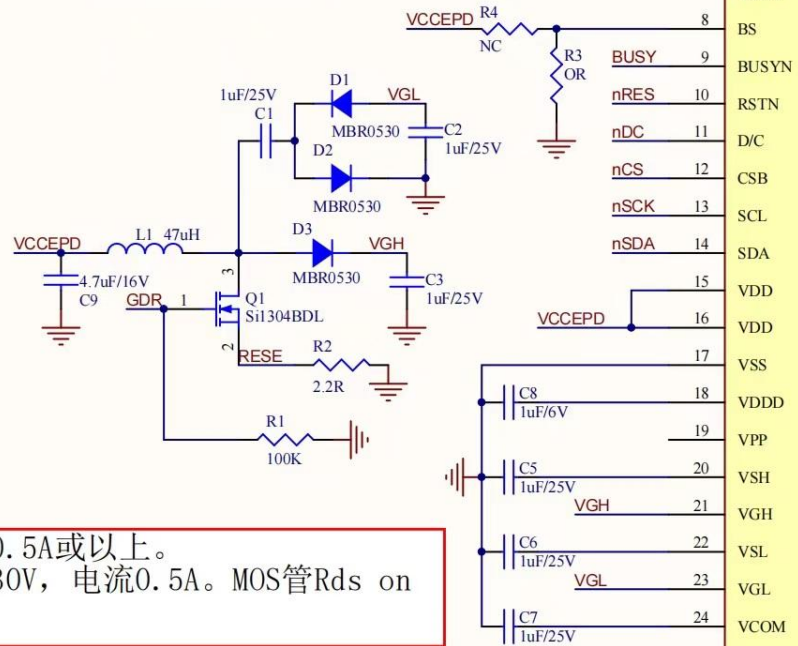
10 Block Diagram



11 Typical Application Circuit with SPI Interface

1. Power Inductor: 47uH, I > 500mA
2. Switch MOS NMOS : V_{ds} ≥ 30V, I_d > 500mA, R_{ds(on)} < 2.1Ω, V_{gs} = 2.5V
3. Schottky Diode: V_r ≥ 30V, I_f > 500mA

EPD DEMO CIRCUIT



- (1) 功率电感用47uH, 电流0.5A或以上。
 (2) MOS管和二极管具: 耐压30V, 电流0.5A。MOS管R_{ds on} ≤ 2.1Ω @ V_{gs} = 2.5V。

EPD_24_INF

12 Inspection Standard

1 目的

规范电子纸模组的检验标准、抽检比例，确保质量符合出货。

2 适用范围

2.1 适用尺寸：≤4.2寸

2.2 产品类型：点阵电子纸显示模组。

3 抽样方案

GB/T 2828.1标准“一般检测水平 II级”“正常检验”进行抽检：

主要缺陷：AQL 0.65（指功能不良或尺寸超出图纸要求，影响装配）

次要缺陷：AQL 1.5（指外观不良，不影响整机功能性能）

4 检查条件

4.1 温度要求：23±3℃；湿度要求：60±15%RH

4.2 检查环境亮度要求：外观检查亮度在700~1000Lux

4.3 检查距离：肉眼距离产品表面35±5cm

4.4 检查角度：眼睛垂直于产品表面，前、后、左、右夹角45°进行检查



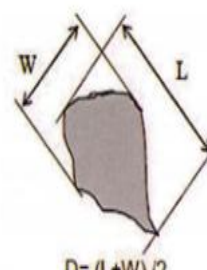
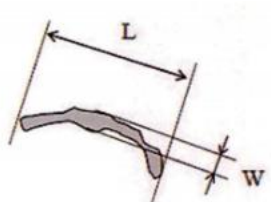
5 定义

5.1 视区定义

A区：显示区域

B区：边缘区域（A区以外的区域）

5.2 点线定义

代码	名称	图示	
N	数量 (个数)	 <p>$D = (L+W)/2$</p> <p>点状图示</p>	 <p>线状图示</p>
L	长度 (mm)		
W	宽度 (mm)		
D	直径 (mm) $D = (L+W)/W$		
DS	点线间距 (mm)		

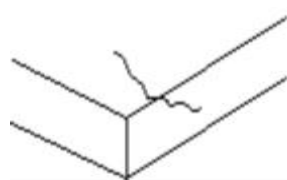
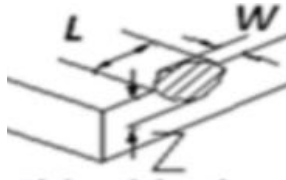
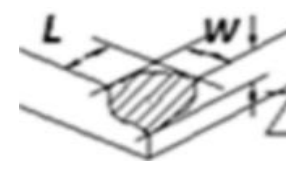
6 检查标准

6.1 主要缺陷 (不允许出现)

序号	检查内容	判定标准
1	显示功能	不显示
		缺划不良
		显示异常
		进水汽
2	外围尺寸	尺寸不符合图纸要求

6.2 主要缺陷 (不允许出现)

序号	检查内容	判定标准		
		点尺寸	A区允许标准	B区允许标准
1	点状、异物、汽泡不良、凹痕、凸痕	$D \leq 0.15\text{mm}$	忽略 (但不可有串污)	忽略
		$0.15\text{mm} \leq D \leq 0.4\text{mm}$	3	
		$D > 0.4\text{mm}$	0	
2	线状异物、刮伤	$W \leq 0.05\text{mm}$	忽略	忽略
		$0.05 < W \leq 0.1\text{mm}$ $L \leq 5.0\text{mm}$	3	
		$W > 0.1\text{mm}$ 或 $L > 5\text{mm}$	不允许	
3	TFT玻璃不良	角	$L < 0.5\text{mm}$; $W < 0.5\text{mm}$ $Z < \text{玻璃厚度}$	允许2处
		边	$L \cong 5\text{mm}$; $W \cong 0.5\text{mm}$; $Z < \text{玻璃厚度}$	每边允许1处
		①.所有破损不允许伤及ITO走线 ②.延伸性的裂缝不允许		

 延伸性裂缝图		 崩边图示		 崩角图示	
4	胶类不良	检查项目	判定标准		
		封边胶高度	1、覆盖四周，不能出现断胶 2、不能出现ITO走线外露 3、胶高度参照图纸要求		
5	FPC	1、金手指粘胶不允许 2、FPC破损不允许			
6	字唛	字体模糊不允许 缺少内容不允许			
7	脏污	1、表面保护膜脏污忽略 2、背面不可出现凸起的异物（如粘胶）等			
8	翘曲度	使用塞规在平整大理石面测量，翘曲度 $\leq 0.8\text{mm}$			

注：

- 1、以上不良按最终显示画面为准，所有画面变换过程屏动的现象不作管控。
- 2、点、线缺陷间距需 $\geq 2\text{mm}$
- 3、背面缺陷不存在可靠性问题的忽略不计