

BU01 Specification

Version V1.0

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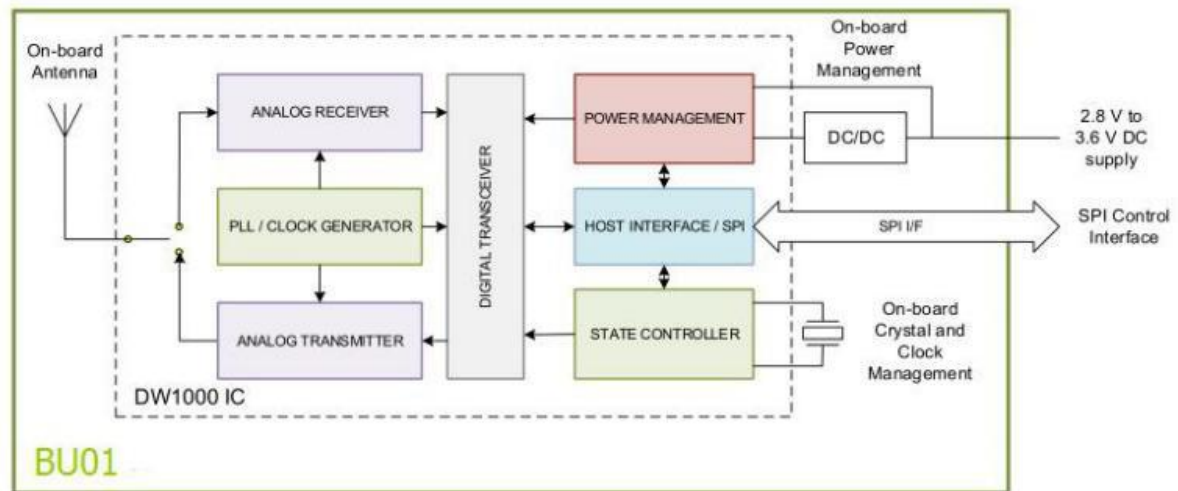
Document development / revision / revocation resume

Version	Date	Develop / revise content	Maker	Verify
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1.Product Overview



BU01 is an ultra wideband (UWB) transceiver module based on Decawave's DW1000 design. BU01 integrates antenna, RF circuit, power management and clock circuit. BU01 can be used in two-way ranging or TDOA positioning system, positioning accuracy can reach 10 cm, and supports data rates up to 6.8 Mbps.

Features

- Simple integration without RF design
- Using RTLS infrastructure to expand communication range
- Super multipath fading has strong anti-interference ability
- Support high label density
- Compliant with IEEE 802.15.4-2011 UWB standard
- Supports 3.5 GHz to 6.5 GHz operating frequency band
- Programmable transmit power
- Power 2.8 V to 3.6 V
- Power consumption <1mA in sleep mode
- Support two-way ranging and TDOA
- Support SPI interface
- Data rate: 110 kbps, 850 kbps, 6.8 Mbps

Main parameters

List 1 specification

Model name	BU01
Size	23*13*2.9(±0.2)MM
Antenna	PCB antenna
Frequency range	3.5 GHz to 6.5 GHz
Working temperature	-40 °C ~ 85 °C
Storage temperature	-40 °C ~ 125 °C , < 90%RH
Power	2.8V ~ 3.6V, default 3.3V, current >200mA
Interface	SPI

2.Electrical parameters

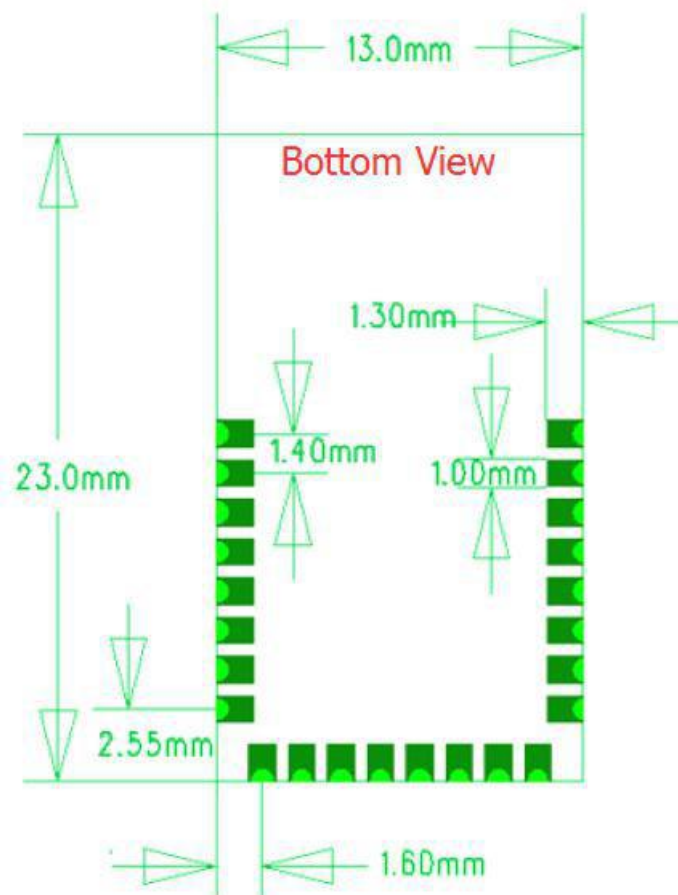
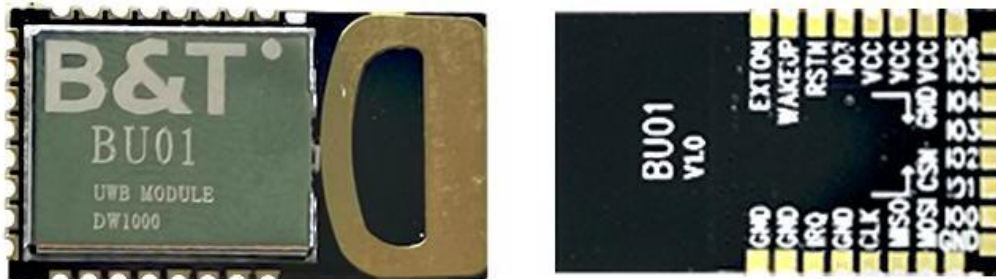
Electrical character

Parameter		Condition	Min	Typical	Max	Unit
Voltage		VDD	2.8	3.3	3.6	V
I/O	V_{IL}/V_{IH}	-	-0.3/0.75VIO	-	0.25VIO/3.6	V
	V_{OL}/V_{OH}	-	N/0.8VIO	-	0.1VIO/N	V
	I_{MAX}	-	-	-	12	mA

RF performance

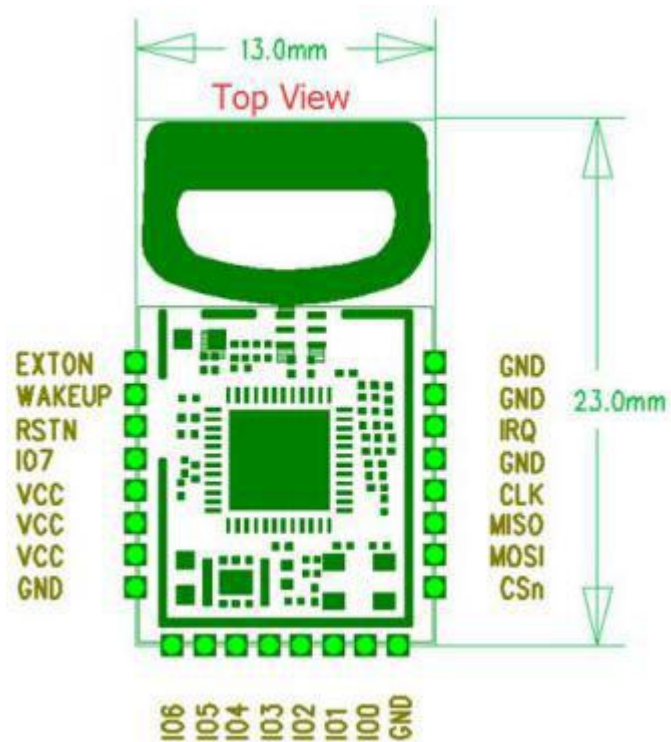
Description	Typical	Unit
Working frequency	3.5 to 6.5	GHz

3.DIMENISON



4. PIN DEFINITION

The BU01 module has a total of 24 interfaces. For example, the pin diagram, the pin function definition table is the interface definition.



BU01 Pin diagram

List PIN function definition

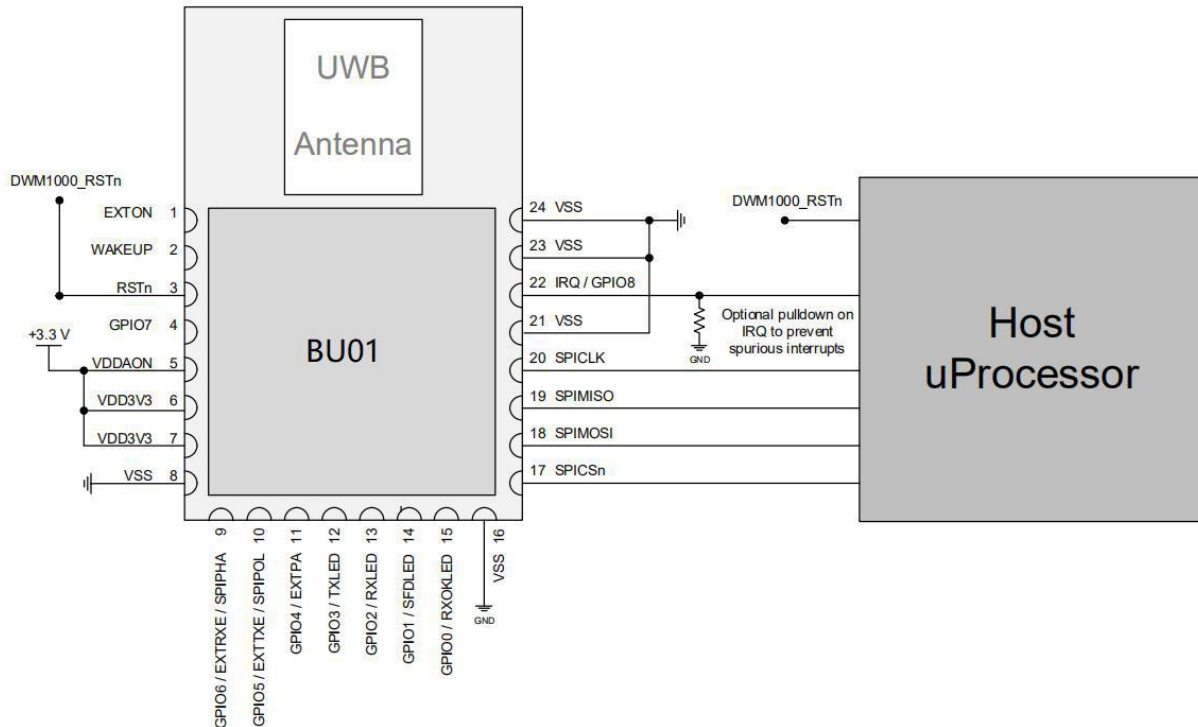
PIN No.	Name	Function description
1	EXTON	The external device is enabled. Asserted and remains active during wake-up until the device enters sleep mode. Can be used to control external DC-DC converters or other circuits that are not needed when the device is in sleep mode to minimize power consumption. For more details, please refer to the DW1000 data sheet
2	WAKEUP	When set to the active high state, the WAKEUP pin brings the DW1000 from sleep or DEEPSLEEP state into working mode. If not used, this pin can be grounded.
3	RSTn	Reset pin. Active low output. Can be pulled low by an external open-drain driver to reset
4	IO7	The default value is used as the SYNC input. This pin can be reconfigured as a general purpose I / O pin GPIO7 under

		software control.
5	VCC	3.3 V power
6	VCC	3.3 V power
7	VCC	3.3 V power
8	GND	Ground
9	IO6	General purpose I / O pin. At power-up, it is used as the SPIPHA (SPI Phase Select) pin to configure the SPI operating mode. After power-up, this pin will default to a general-purpose I / O pin.
10	IO5	General purpose I / O pin. At power-up, it is used as an SPIPOL (SPI Polarity Select) pin to configure the SPI operating mode. After power-up, this pin will default to a general-purpose I / O pin.
11	IO4	Universal I / O PIN.
12	IO3	General purpose I / O pin. It can be configured to be used as a TXLED drive pin, which can be used to light the LED after transmission.
13	IO2	General purpose I / O pin. It can be configured as a RXLED drive pin, which can be used to light the LED in receive mode.
14	IO1	General purpose I / O pin. It can be configured to be used as an SFDLED drive pin, which can be used to light the LED when the receiver finds an SFD (Start Frame Delimiter).
15	IO0	General purpose I / O pin. It can be configured as a RXOKLED drive pin, which can be used to light the LED after receiving a good frame.
16	GND	Ground
17	CSn	SPI chip selection. This is an active-low enable input. A high-to-low transition on SPICSn indicates the start of a new SPI transaction. SPICSn can also be used as a wake-up signal to bring the DW1000 out of sleep or sleep.
18	MOSI	SPI data input
19	MISO	SPI data output
20	CLK	SPI clock
21	GND	Ground

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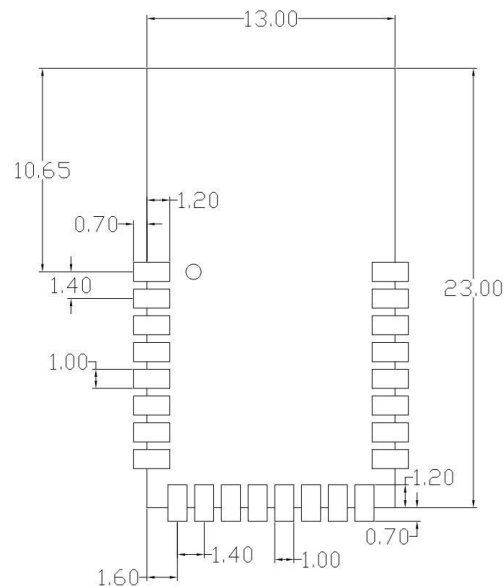
6.DESIGN GUIDE

1、Application circuit



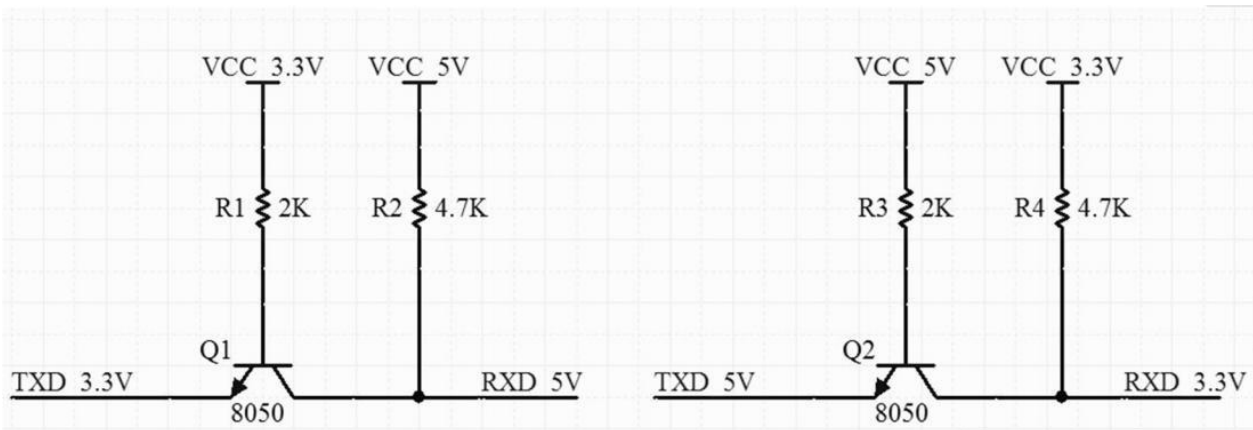
2、Recommended module package design size

Note: Below is the BU01 module package diagram, it is recommended to design the PCB board according to this diagram, so that the module can work normally on the PCB board; and pay attention to the design of the pad, the design of the pads on the PCB can not be offset from the corresponding pads of the module, and the expansion of the PCB pads relative to the module pads does not affect the use of the module.



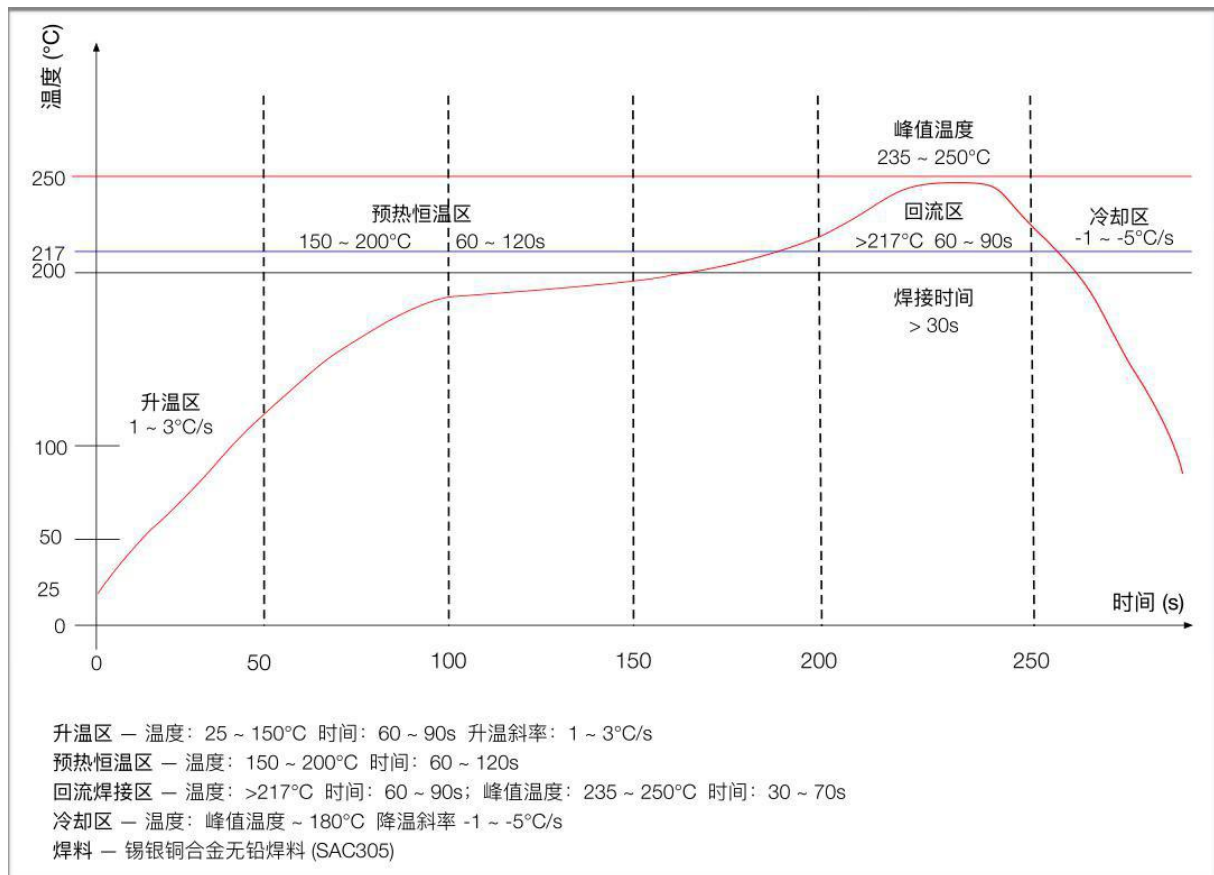
5、USE of GPIO port

- (1) There are some GPIO ports on the periphery of the module. If you need to use a 10-100 ohm resistor in series with the IO port, it is recommended. This can suppress overshoot, and the levels on both sides are more stable. Used for both EMI and ESD.
- (2) The special IO port is pulled up and down, please refer to the instruction manual of the specification, this will affect the startup configuration of the module.
- (3) The IO port of the module is 3.3V. If the IO level of the main control and the module does not match, a level conversion circuit needs to be added.
- (4) If the IO port is directly connected to a peripheral interface, or a pin or other terminal, it is recommended to reserve an ESD device near the terminal of the IO trace.



List Level-shifting circuit

7. REFLOW PROFILE



8.PACKAGING

As shown below, the packing of BU01 is taping.

