

nRFLR2021

Wireless Communication Module Specification

**nRF52840 + Semtech LR2021 Sub-GHz + 2.4 GHz Dual-Band
Module**

Version: V1.0

Release Date: 2026/09/10

Hardware Version: nRFLR2021_V1.0

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1. Overview

1.1 Description

nRFLR2021 is a dual-core wireless communication module that integrates Nordic Semiconductor's nRF52840 Bluetooth Low Energy / Thread / Zigbee multiprotocol SoC with Semtech's fourth-generation LoRa Plus™ LR2021 dual-band transceiver. In a single QFN-32 chip, the LR2021 simultaneously supports a Sub-GHz (150–960 MHz) and a 2.4 GHz ISM (1.5–2.5 GHz) RF front end, plus a 1.6–2.4 GHz satellite S-Band (LR-FHSS) interface, covering multiprotocol applications including LoRaWAN, LoRa point-to-point, BLE PHY, FLRC, O-QPSK 802.15.4, Amazon Sidewalk, Wi-SUN, Wireless M-Bus, Sigfox BPSK, and Z-Wave.

The module integrates a 32 MHz industrial-grade TCXO reference clock, LR2021 internal SIMO/LDO power management and Direct-Tie switchless RF matching front end, and two antenna ports (ANT_LORA shared by Sub-GHz and 2.4 GHz)). The host nRF52840 directly controls the LR2021 via SPI, and provides USB 2.0 Full-Speed, SWD debugging, and full-function GPIOs for rapid integration into battery-powered and high-density IoT terminal products.

1.2 Key Features

- Highly integrated dual-core architecture: nRF52840 (Cortex-M4F @ 64 MHz, BLE 5.4 / Thread / Zigbee) + LR2021 (Sub-GHz + 2.4 GHz dual-band LoRa Plus), integrating an MCU and dual-band multiprotocol wireless on a single board.
- Long-range Sub-GHz communications: 150~960 MHz, maximum transmit power of +22 dBm, LoRa receive sensitivity of –141.1 dBm (SF12/125 kHz), and a typical link budget of 163 dB.
- Integrated 2.4 GHz RF: 1.5–2.5 GHz band, BLE 5.0 PHY (–100 dBm @ 1 Mbps), FLRC (2.6 Mbps), O-QPSK 802.15.4, and S-Band LR-FHSS satellite communications.
- Dual-antenna design: ANT_LORA (Sub-GHz + 2.4 GHz, single-port Direct-Tie switching), simplifying integration and certification layout.

- BLE 5.4 / Thread / Zigbee: The nRF52840 natively supports Bluetooth 5.4 Direction Finding, Thread 1.3, Zigbee 3.0, NFC-A, and near-field commissioning.
- Industrial-grade TCXO reference: 32 MHz TCXO (NX2016SA-32M-EXS00A) + 32.768 kHz RTC crystal, with LR2021 frequency stability < 1.5 ppm.
- Ultra-low power: nRF52840 system-level power consumption as low as ~0.3 μ A in System OFF mode; LR2021 typical current of 583 nA in Deep-sleep mode (without RTC).
- PackageDimensions: 20 × 20 × 3.5 mm, 80-pin, SMT, LGA package, 1 mm board thickness;
- Rich interface resources: USB 2.0 Full-Speed, SWD, 48 GPIOs, I²C/SPI/UART/PWM/QDEC/PDM, 12-bit ADC, and an independent NFC-A tag.
- Industrial temperature range: -40 °C to +85 °C operation, designed and targeted for RoHS / REACH environmental compliance and certification.

1.3 Applications

- Smart metering: electricity, water, gas, and heat meters, supporting LoRaWAN Sub-GHz and 2.4 GHz dual links; BLE near-field meter reading.
- Asset tracking: Sub-GHz outdoor backhaul + 2.4 GHz indoor positioning dual links, creating a hybrid-positioning asset network.
- Smart agriculture / livestock: soil, weather, and livestock sensors, with multi-year battery-powered deployment, supporting LoRaWAN + FLRC.
- Smart home / building: compatible with Sidewalk / Z-Wave / Thread; can serve as a border router or end node.
- Industrial IoT: predictive equipment maintenance, environmental monitoring, and factory mesh networking (FLRC high-speed links).
- Emergency and outdoor: mesh intercoms, positioning beacons, and remote synchronization for wearable devices.
- Satellite IoT: interfaces with S-Band LR-FHSS for direct connection to low-Earth-orbit satellite IoT networks.
- AIoT edge nodes: the nRF52840 can run lightweight ML inference (TFLite Micro), combined with Sub-GHz / 2.4 GHz dual-link backhaul.

2. System Block Diagram

The nRFLR2021 module uses the Nordic nRF52840 SoC as the host MCU and connects to the Semtech LR2021 dual-band transceiver through an SPI bus. The LR2021 integrates Sub-GHz PA/LNA, 2.4 GHz PA/LNA, an S-Band interface, SIMO/LDO power management, and baseband modulation/demodulation. ANT_LORA is multiplexed between Sub-GHz and 2.4 GHz through a Direct-Tie (RF-switchless) matching network; an independent satellite RF front end may be connected externally.

The 32 MHz TCXO provides the LR2021 with a precision reference clock (frequency offset < 1.5 ppm); the nRF52840 includes its own 2.4 GHz BLE RF (no independent ANT_BLE port is brought out in V1.0), for BLE / Thread / Zigbee communications or near-field commissioning.

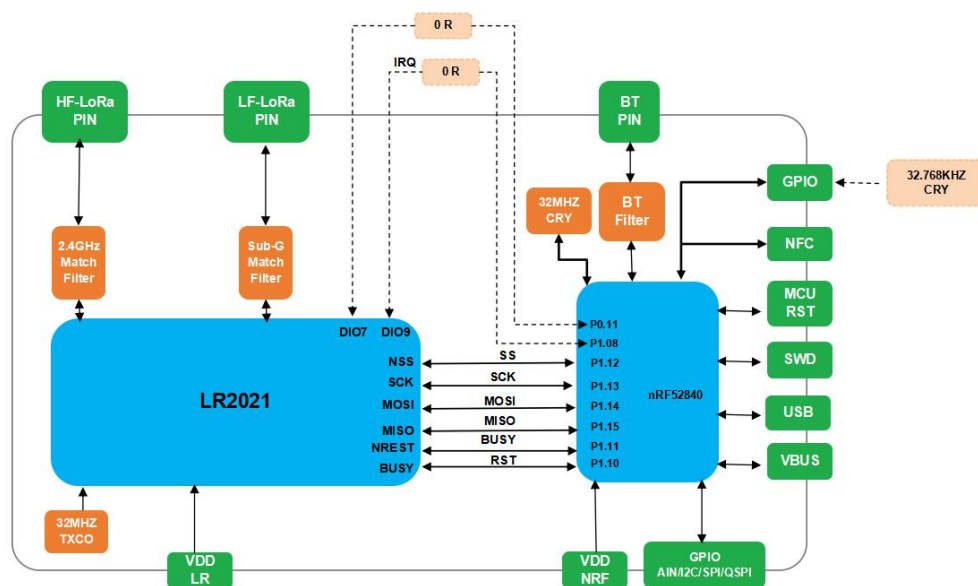


Figure 1 nRFLR2021 Module System Block Diagram

3. Hardware Overview

3.1 Board Layout

The nRFLR2021 module uses an 80-pad SMT LGA package, with 20 pads on each of the four sides (80 total). Each pad measures 1.2×0.5 mm, with approximately 0.92 mm center-to-center spacing between adjacent pads; the module's external dimensions, including protruding pads, are approximately 19 mm $\times$ 19 mm $\times$ 2.5 mm. The top side primarily contains the nRF52840 SoC (U4), LR2021 transceiver (U5, QFN32), 32 MHz TCXO reference clock, RF Direct-Tie matching network, and decoupling capacitors; the bottom side contains SMD pads and external antenna routing.

The antenna ports use Direct-Tie (RF-switchless), single-ended 50 Ω interfaces: ANT_LORA (pin 72) is the multiplexed Sub-GHz + 2.4 GHz port. Both antenna paths are directly coupled to the LR2021 internal PA/LNA through π matching networks; no additional RF switch is required on the PCB.

3.2 Pin Definitions

nRFLR2021-Pin Definition

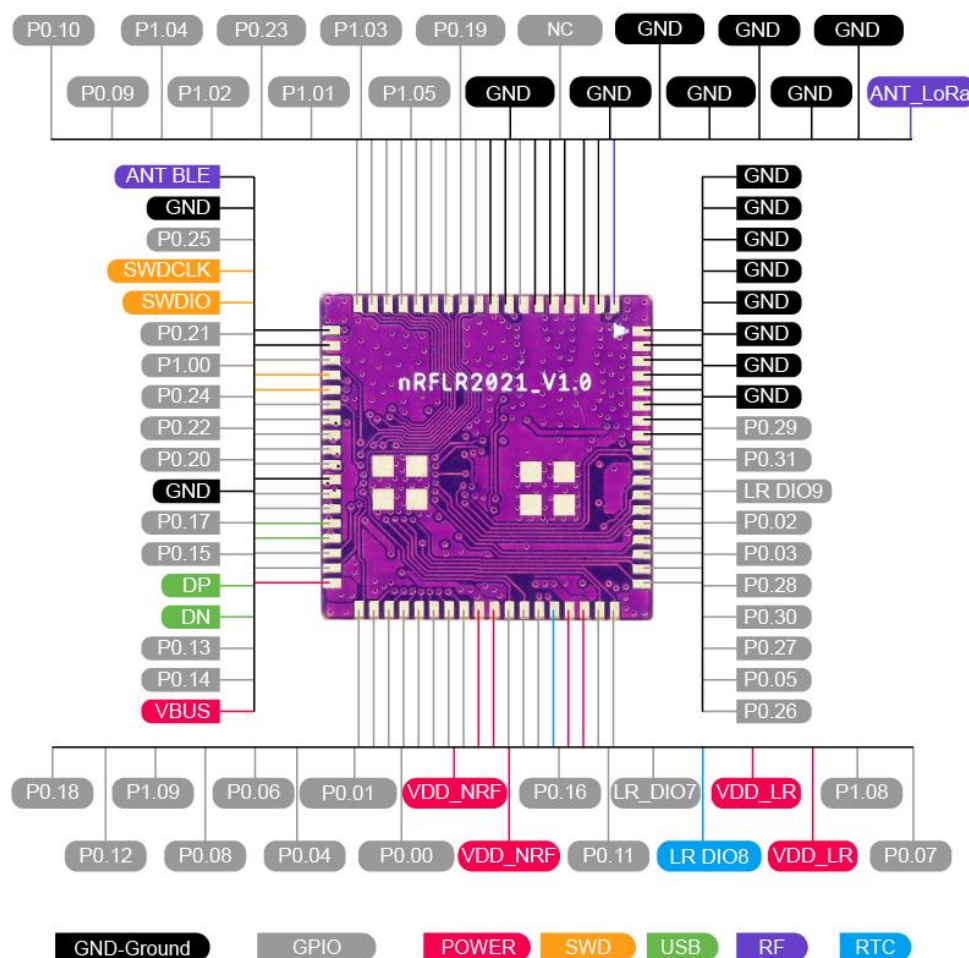


Figure 2 nRFLR2021 Module Pin Definitions (80-Pad)

The following table lists the pad (U5, SMD80) pin definitions for the nRFLR2021 module. Decoupling capacitors should be placed close to all power and GND pins to reduce supply ripple. All GPIO ports default to nRF52840 GPIOs and can be flexibly configured in firmware; pin numbers such as VDD_NRF_27/28 and VDD_LR_21/22 are marked by the U5 reference designator.

Table 1 nRFLR2021 Module Pin Definitions (80-Pad, SMD80 Footprint)

No.	Name	Type	Function Description
1	GND	—	System ground
2	GND	—	System ground
3	GND	—	System ground
4	GND	—	System ground
5	GND	—	System ground
9	P0.29/AIN5	I/O	nRF52840 GPIO / analog input
10	P0.31/AIN7	I/O	nRF52840 GPIO / analog input
11	LR_DIO9	I/O	LR2021 DIO9 multifunction digital I/O
12	P0.02/AIN0	I/O	nRF52840 GPIO / analog input
13	P0.03/AIN1	I/O	nRF52840 GPIO / analog input
14	P0.28/AIN4	I/O	nRF52840 GPIO / analog input
15	P0.30/AIN6	I/O	nRF52840 GPIO / analog input
16	P0.27	I/O	nRF52840 GPIO
17	P0.05/AIN3	I/O	nRF52840 GPIO / analog input
18	P0.26	I/O	nRF52840 GPIO
19	P0.07	I/O	nRF52840 GPIO
20	P1.08	I/O	nRF52840 GPIO
21	VDD_LR_22	Power	LR2021 supply (1.8 V – 3.7 V, typ. 3.3 V); 4.7 μ F + 100 nF decoupling in parallel recommended
22	VDD_LR_21	Power	LR2021 supply, connected in parallel with pin 21
23	LR_32K_OUT	O	LR2021 32 kHz reference output (optional, for RTC)
24	LR_DIO7	I/O	LR2021 DIO7 multifunction digital I/O
25	P0.11	I/O	nRF52840 GPIO
26	P0.16	I/O	nRF52840 GPIO
27	VDD_NRF_27	Power	nRF52840 supply (1.7 V – 5.5 V, typ. 3.3 V / 5 V); 10 μ F + 100 nF in parallel recommended
28	VDD_NRF_28	Power	nRF52840 supply, connected in parallel with pin 27
29	P0.00/XL1	I/O	nRF52840 GPIO / 32.768 kHz crystal interface 1
30	P0.01/XL2	I/O	nRF52840 GPIO / 32.768 kHz crystal interface 2
31	P0.04/AIN2	I/O	nRF52840 GPIO / analog input
32	P0.06	I/O	nRF52840 GPIO
33	P0.08	I/O	nRF52840 GPIO
34	P1.09	I/O	nRF52840 GPIO
35	P0.12	I/O	nRF52840 GPIO
36	P0.18/NRESET	I/O	nRF52840 GPIO / internal NRESET routing (external 100

No.	Name	Type	Function Description
			kΩ pull-up recommended)
37	VBUS	Power	USB bus power input (5 V); leave floating if USB is not used
38	P0.14	I/O	nRF52840 GPIO
39	P0.13	I/O	nRF52840 GPIO
40	D– (USB)	I/O	USB D– data line
41	D+ (USB)	I/O	USB D+ data line
42	P0.15	I/O	nRF52840 GPIO
43	P0.17	I/O	nRF52840 GPIO
45	P0.20	I/O	nRF52840 GPIO
46	P0.22	I/O	nRF52840 GPIO
47	P0.24	I/O	nRF52840 GPIO
48	P1.00	I/O	nRF52840 GPIO
49	P0.21	I/O	nRF52840 GPIO
50	SWDIO	I/O	ARM SWD data line
51	SWDCLK	I	ARM SWD clock line
52	P0.25	I/O	nRF52840 GPIO
55	P0.10/NFC2	I/O	nRF52840 GPIO / NFC antenna interface 2
56	P0.09/NFC1	I/O	nRF52840 GPIO / NFC antenna interface 1
57	P1.04	I/O	nRF52840 GPIO
58	P1.02	I/O	nRF52840 GPIO
59	P0.23	I/O	nRF52840 GPIO
60	P1.01	I/O	nRF52840 GPIO
61	P1.03	I/O	nRF52840 GPIO
62	P1.05	I/O	nRF52840 GPIO
63	P0.19	I/O	nRF52840 GPIO
67	NC		
72	ANT_LORA	RF I/O	LR2021 main antenna port (Direct-Tie multiplexed Sub-GHz 150–960 MHz and 2.4 GHz 1.5–2.5 GHz), 50 Ω
77	GND	—	System ground
78	GND	—	System ground
79	GND	—	System ground
80	GND	—	System ground

Note: The numbers in the table correspond one-to-one with the pad numbers of the module (U5, SMD80_LR11XX_MO_2X2MM footprint); omitted numbers are unused pads / NC.

4. Technical Specifications

Unless otherwise specified, the following parameters are summarized at VDD_NRF = VDD_LR = 3.3 V, an ambient temperature of 25 °C, and a 32 MHz TCXO reference clock.

Parameter Category	Parameter Name	Parameter Value
Chip and Hardware	Host MCU	Nordic nRF52840, Cortex-M4F @ 64 MHz, 1 MB Flash, 256 KB RAM
Chip and Hardware	Wireless Transceiver	Semtech LR2021 fourth-generation LoRa Plus™ dual-band transceiver (QFN32, 5 × 5 mm)
Chip and Hardware	Reference Clock (Wireless)	NX2016SA-32M-EXS00A industrial-grade 32 MHz TCXO; LR2021 frequency offset < 1.5 ppm
Chip and Hardware	Reference Clock (RTC)	32.768 kHz low-power crystal (external, optional)
Chip and Hardware	Operating Voltage (NRF Domain)	1.7 V ~ 5.5 V, typical 3.3 V / 5 V (USB)
Chip and Hardware	Operating Voltage (LR Domain)	1.8 V ~ 3.7 V, typical 3.3 V; VTCXO (internal) 3.0 V
Chip and Hardware	Operating Temperature	–40 °C ~ +85 °C (industrial grade)
Chip and Hardware	Package Dimensions	Core 18.5 mm × 18.5 mm; external dimensions including protruding pads ≈ 19 mm × 19 mm × 2.5 mm; 80-pad SMT (SMD80 footprint)
Chip and Hardware	Antenna Port	ANT_LORA (Sub-GHz + 2.4 GHz, Direct-Tie)
MCU Interface	USB	USB 2.0 Full-Speed (12 Mbps), VBUS power detection
MCU Interface	Debug	ARM SWD (SWDIO/SWDCLK)

Parameter Category	Parameter Name	Parameter Value
MCU Interface	GPIO	Up to 48 GPIOs, including I ² C / SPI / UART / PWM / QDEC / PDM / 12-bit ADC / NFC-A
MCU Interface	Wireless Protocols	BLE 5.4 (Direction Finding), Bluetooth Mesh, Thread 1.3, Zigbee 3.0, NFC-A
RF (Sub-GHz)	Frequency Band	150 ~ 960 MHz (868 / 915 MHz ISM mainstream)
RF (Sub-GHz)	Maximum Transmit Power	+22 dBm (LF PA)
RF (Sub-GHz)	Transmit Power Dynamic Range	32 dB, 0.5 dB steps
RF (Sub-GHz)	LoRa Receive Sensitivity	-141.1 dBm @ SF12 / BW = 125 kHz
RF (Sub-GHz)	LoRa Data Rate	0.0458 ~ 125 kbps (LoRa modulation)
RF (2.4 GHz)	Frequency Band	1.5 ~ 2.5 GHz ISM
RF (2.4 GHz)	Maximum Transmit Power	+12 dBm (2.4 GHz PA)
RF (2.4 GHz)	LoRa @ 2.4 GHz Sensitivity	-133 dBm @ SF12 / BW = 400 kHz
RF (S-Band)	Frequency Band	1.6 ~ 2.4 GHz (LR-FHSS), -131 dBm sensitivity (S-Band)
RF (nRF52840)	2.4 GHz Transmit Power	-20 ~ +8 dBm, programmable
RF (nRF52840)	BLE Receive Sensitivity	-96 dBm @ 1 Mbps BLE
Modulation	Sub-GHz Modulation	LoRa / (G) FSK / MSK / BPSK (Sigfox) / OOK / O-QPSK / LR-FHSS
Modulation	2.4 GHz Modulation	LoRa / (G) FSK / FLRC (≤ 2.6 Mbps) / O-QPSK (802.15.4) / BLE 5.0 PHY
Modulation	Spreading Factor (LoRa)	SF5 ~ SF12
Interface (Wireless)	MCU ↔ LR2021 Bus	SPI (≤ 16 MHz, Mode 0) + DIO/BUSY/NRESET handshake
Interface (Wireless)	LR2021 DIO Channels	Seven channels, DIO5 ~ DIO11 (no DIO0 ~ DIO4)
Interface (Wireless)	LR2021 Data FIFO	Independent TX / RX FIFOs

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings below may cause permanent damage to the device. Extended operation under absolute maximum rating conditions may affect device reliability and service life.

Symbol	Description	Minimum	Maximum	Unit
VDDmr_NRF	nRF52840 supply voltage	−0.3	5.5	V
VDDmr_LR	LR2021 supply voltage (VCC)	−0.5	3.9	V
VBUSmr	USB VBUS voltage	−0.3	5.8	V
Tmr_store	Storage temperature	−40	+125	°C
PMR_RF	ANT_LORA / Maximum input power	—	+10	dBm
VESD_HBM	ESD (HBM, all pins)	—	±2000	V
VESD_CDM	ESD (CDM, all pins)	—	±500	V

Note: The LR2021 uses a Direct-Tie (RF-switchless) matching network, with the PA output (RFO) and LNA input (RFI) sharing the same RF node. Any external power applied to the antenna port appears simultaneously at the RFI and RFO ports. +10 dBm is a stress-level rating; operation at +6 dBm or above may affect device reliability. External power above +6 dBm requires additional front-end protection.

5.2 Normal Operating Conditions

Symbol	Description	Minimum	Typical	Maximum	Unit
VDD_NRF	nRF52840 supply	1.7	3.3 / 5.0	5.5	V
VDD_LR	LR2021 supply (VCC)	1.8	3.3	3.7	V
VTCXO	LR2021 internal VTCXO LDO	—	3.0	—	V
VBUS	USB bus voltage	4.4	5.0	5.25	V
Top	Operating temperature	−40	—	+85	°C
Tstore	Storage temperature	23 ± 5 (recommended)	—	+125	°C
Tmaxj_NRF	nRF52840 maximum junction	—	—	+125	°C

Symbol	Description	Minimum	Typical	Maximum	Unit
	temperature				
Tmaxj_LR	LR2021 maximum junction temperature	—	—	+105	°C
VSWR	Voltage standing-wave ratio for guaranteed PA stability	—	—	10:1	—
Vripple_LR	VDD_LR ripple (BW=20 MHz)	—	11.2	—	mV
Vripple_TCXO	VTCXO ripple (BW=20 MHz)	—	8.13	—	mV

5.3 Power Consumption Parameters

The power consumption values in the following table are typical device-level values; the nRF52840 and LR2021 are controlled independently. System-level power consumption is the sum of the operating modes of both devices. Power consumption for the Sub-GHz and 2.4 GHz bands is listed separately.

Module	Mode	Condition	Typical	Unit
nRF52840	System ON, Sleep	RAM retention + RTC running	1.9	μA
nRF52840	System OFF	No RAM retention, no RTC	0.3	μA
nRF52840	CPU running	Cortex-M4F @ 64 MHz, CoreMark	7.5	mA
nRF52840	Radio TX (BLE)	0 dBm, DC-DC mode	5.3	mA
nRF52840	Radio RX (BLE)	1 Mbps BLE	5.4	mA
LR2021	Deep Sleep	No data retention, no RTC	583	nA
LR2021	Idle / Standby	Internal RC oscillator retained (chip-level)	960	μA
LR2021	Standby XOSC	32 MHz TCXO enabled	1.79	mA
LR2021	TX Sub-GHz +10 dBm	868 / 915 MHz	19.4	mA
LR2021	TX Sub-GHz +14 dBm	868 MHz	38.5	mA
LR2021	TX Sub-GHz +17 dBm	868 / 915 MHz	52.3	mA
LR2021	TX Sub-GHz +20 dBm	868 / 915 MHz	92.5	mA
LR2021	TX Sub-GHz +22 dBm	868 MHz	116.0	mA
LR2021	TX Sub-GHz +22	915 MHz	119.4	mA

Module	Mode	Condition	Typical	Unit
	dBm			
LR2021	TX 2.4 GHz +0 dBm	BLE PHY / FLRC	13.6	mA
LR2021	TX 2.4 GHz +12 dBm	BLE PHY / FLRC	28.4	mA
LR2021	RX Sub-GHz LoRa	SF12 / 125 kHz	8.19	mA
LR2021	RX 2.4 GHz LoRa	SF12 / 125 kHz	8.59	mA
LR2021	RX Sub-GHz FLRC	260 kbps	7.99	mA
LR2021	RX 2.4 GHz FLRC	260 kbps	8.52	mA

Note: The above power consumption values are typical device data; actual system power consumption varies with peripheral circuitry, firmware implementation, and operating duty cycle. Use measured results for system-level power evaluation. The LR2021 provides Sub-GHz and 2.4 GHz dual-band PAs and can perform cross-band switching on a single chip; the Direct-Tie architecture significantly reduces RF path loss and BOM complexity.

6. Mechanical Characteristics

6.1 Board Dimensions

nRFLR2021 The module outline dimensions and PCB layout recommendations are shown in Figure 3. The module uses the same 20.0 mm × 20.0 mm × 3.5 mm LGA package as the nRFLR2012 module, with an 18.5 mm × 18.5 mm PCB core, 1.0 mm PCB thickness, 72 peripheral pads (18 per side) + 8 central thermal pads. Four M2 mounting holes are located at the four corners of the board, allowing the module to be secured with copper standoffs or screws.

The module package geometry and land pattern are fully compatible with nRFLR2012.

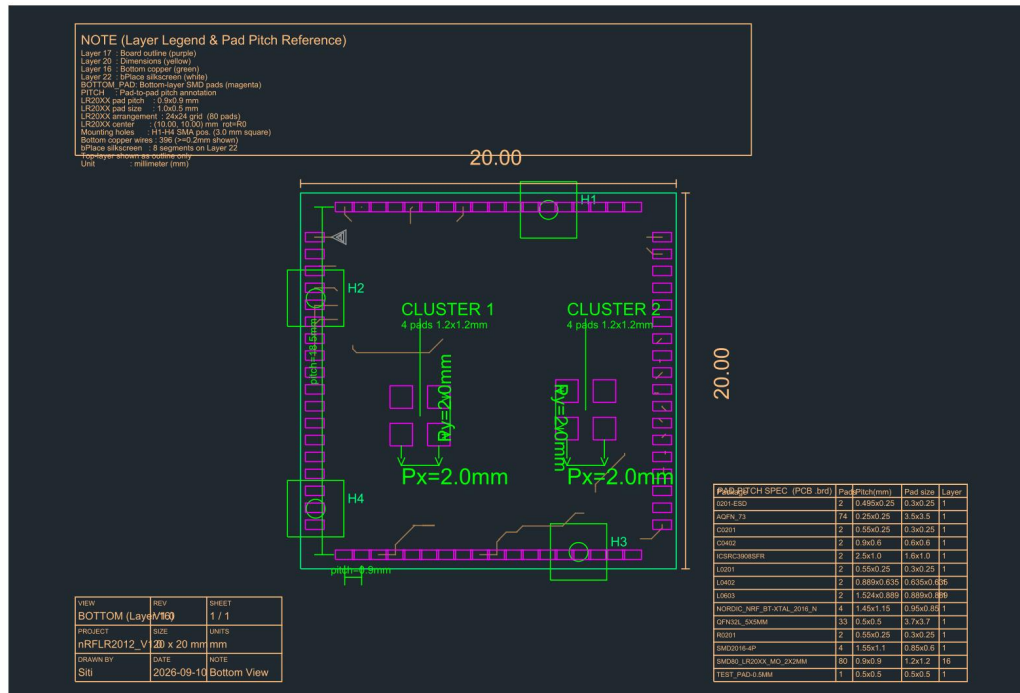


Figure 3 nRFLR2021 Module Outline Dimensions (Unit: mm)

Item	Value	Tolerance	Unit	Notes
Core length	18.5	±0.15	mm	SMD80 footprint pad boundary
Core width	18.5	±0.15	mm	SMD80 footprint pad boundary
PCB thickness	1.0	±0.10	mm	4-layer board, 1 oz copper
Total module thickness	2.5	±0.20	mm	Including pad protrusion
Module external dimensions (reference)	19 × 19	±0.20	mm	Including pad protrusion
Pad width (X direction)	1.20	±0.05	mm	Recommended SMD process value
Pad length (Y direction)	0.50	±0.05	mm	Recommended SMD process value
Pad center spacing	0.92	±0.05	mm	20 pads evenly distributed on each of the four sides
SMDPad count	80	—	PCS	20 pads on each side
SMDCenter position	(10, 10)	—	mm	EAGLE board coordinate

Item	Value	Tolerance	Unit	Notes
				system, relative to the BRD origin

6.2 Layout Recommendations

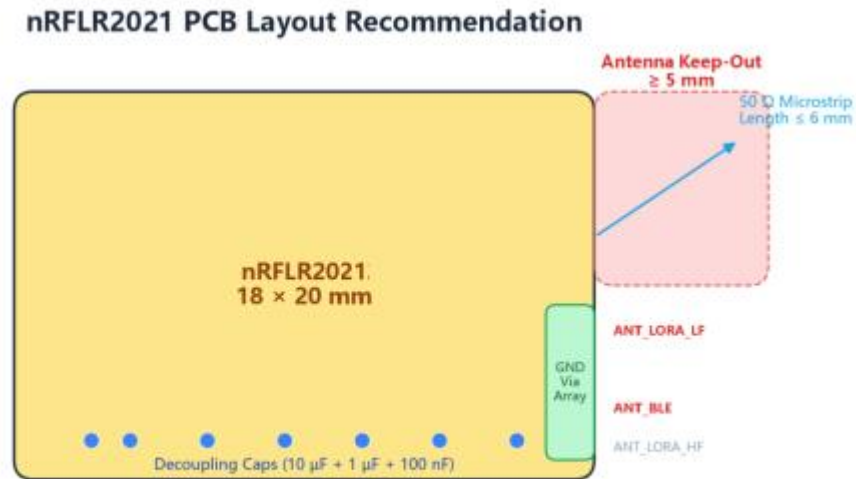


Figure 4 nRFLR2021 PCB Layout Recommendations (Unit: mm)

PCB layout considerations:

- Do not place copper or traces beneath the antenna port. Reserve at least a 5 mm clearance area around ANT_LORA to reduce parasitic capacitance and impedance mismatch.
- ANT_LORA traces should maintain a 50 Ω characteristic impedance, have a length ≤ 6 mm, and be flanked on both sides by arrays of ground vias (spacing ≤ 1 mm).
- The LR2021 uses switchless Direct-Tie matching internally, with RFO and RFI sharing the same node. The π matching network (L/C components) on the module should be placed close to the U5 pins, with the return path as short and wide as possible.
- The 32 MHz TCXO traces should be surrounded by ground, with ground vias placed on both sides of the signal traces, and routed away from high-frequency switching power paths; TCXO power is supplied by the LR2021 internal 3.0 V LDO.

- Place power decoupling capacitors close to the VDD_NRF / VDD_LR pins.
Recommended values are 10 μ F + 1 μ F + 100 nF on VDD_NRF and 4.7 μ F + 1 μ F + 100 nF on VDD_LR.
- For the nRF52840 and LR2021 SPI traces, a 470 Ω series resistor is recommended on the SPI bus (placed close to the module) to suppress signal reflections and EMI.
- USB D+/D– differential traces should maintain a 90 Ω differential impedance, have ground vias on both sides, and avoid crossing plane splits.
- Connect the module bottom pads to the main ground plane through multiple vias to ensure good grounding and heat dissipation.
- If USB is not used, leave the VBUS pin floating to prevent abnormal startup caused by unintended USB power-up.

7. Reference Schematic

Figure 5 shows the typical application reference schematic for the nRFLR2021 module (nRFLR2021_V1.0). This reference design includes a 3.3 V power tree, nRF52840 host circuit, LR2021 Sub-GHz / 2.4 GHz / S-Band Direct-Tie RF front end, SPI connections and control handshaking, TCXO and crystal, ANT_LORA / matching network, and decoupling circuitry.

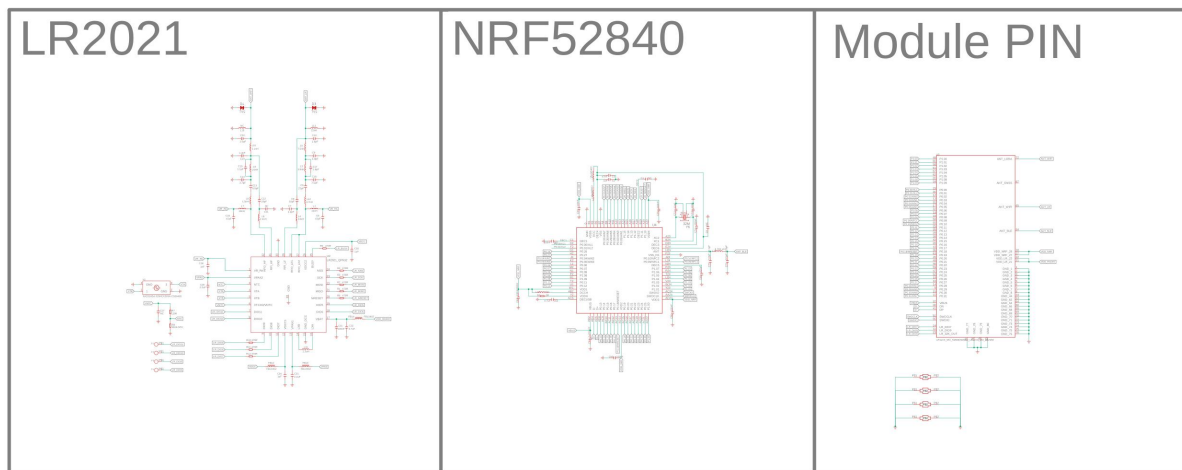


Figure 5 nRFLR2021 Module Reference Schematic (nRFLR2021_V1.0)

Key schematic design points:

- The VDD_LR input is recommended to use multilayer decoupling with $4.7\ \mu\text{F} + 1\ \mu\text{F} + 100\ \text{nF}$; the VDD_NRF input is recommended to use multilayer decoupling with $10\ \mu\text{F} + 1\ \mu\text{F} + 100\ \text{nF}$.

- It is recommended to place a 470 Ω series resistor on the SPI bus (NSS/SCK/MOSI/MISO) to suppress high-order harmonics; add a 100 k Ω pull-up on MISO to prevent the bus from floating.
- LR_NRESET is recommended to be connected to VDD_LR through a 100 k Ω pull-up resistor to ensure a stable reset pin. LR_BUSY can be directly connected to an nRF52840 GPIO as a handshake signal.
- The 32 MHz TCXO (NX2016SA-32M-EXS00A) is connected through the XTA/XTB pins of the LR2021; the TCXO power is provided by the LR2021's internal 3.0 V VTCXO LDO.
- The ANT_LORA design uses a 50 Ω π -type matching network covering both the Sub-GHz (150–960 MHz) and 2.4 GHz (1.5–2.5 GHz) bands; U5 uses internal Direct-Tie switching, so no external RF switch is required.
- It is recommended to add an ESD protection device (such as a TVS diode) to the ANT_LORA port to enhance the system's electrostatic protection.
- The nRF52840 SWD interface (SWDIO/SWDCLK) is recommended to use a 100 Ω series resistor plus a 100 k Ω pull-down resistor to protect the debugging interface.
- For the USB interface, it is recommended to add a 22 Ω series resistor and an ESD protection array (TVS) on each of D+ and D– to meet the IEC 61000-4-2 ± 8 kV contact discharge requirement.
- The nRF52840's built-in 2.4 GHz radio is used for BLE / Zigbee / Thread; the V1.0 module does not expose a separate ANT_BLE_SMD port, allowing the OEM motherboard to expand flexibly through GPIO + a π matching network.

8. Certification

FCC / CE / RoHS certification.

9. Ordering Information

Technical Support: techsupport@elecrow.com

Sales: info@elecrow.com

10. Related Documents and Resources

- [➤Link](#)

11. Revision History

Date	Version	Release Notes
2026/09/10	V1.0	Initial release.